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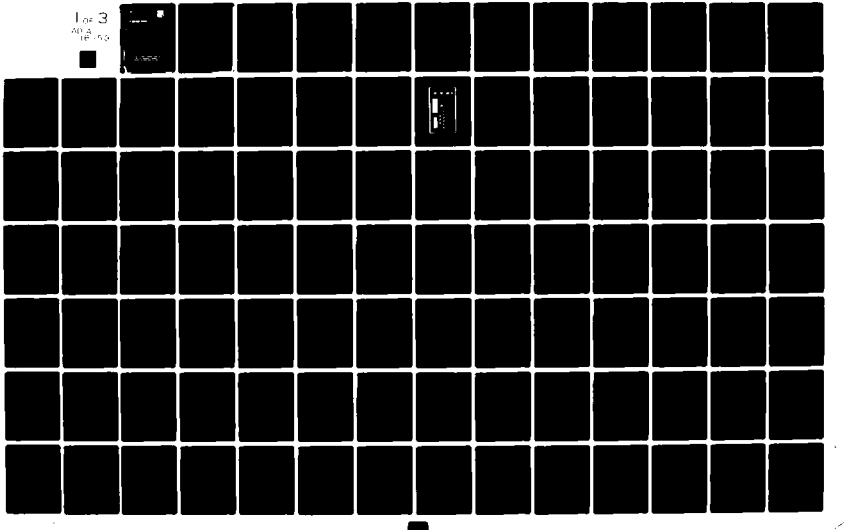

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Final Technical Report
April 1982

HF WIDEBAND MODEM

GTE Sylvania

Victor Ellins, Peter H. Anderson and Mark N. Sandler

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ROME AIR DEVELOPMENT CENTER
Air Force Systems Command
Griffiss Air Force Base, NY 13441

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This was an engineering effort to design, simulate, implement and test two HF modems capable of sustaining data rates of 4800 b/s or greater over standard 3 kHz HF channels. The first twelve months of effort encompassed propagation analysis, modulation waveform parameter selection overall modem and decision feedback equalizer (DFE) design, error control study, computer simulation, and real-time hardware and software design tasks. Subsequent work included the real-time modem implementation,

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preliminary (factory) acceptance testing and final (RADC DICEF) acceptance testing tasks. Also an initial live link test was included. The two identical high data rate HF modem (HFWBM) terminals offer reliable data communication at rates above 1 b/s/Hz over practical HF radio circuits. The characteristics and performance of the HFWBM have been shown to meet or exceed all contract specifications. Under the contract operation at 2400 b/s and 4800 b/s were requirements, while operation at 9600 b/s in a 3 kHz channel was stated as a design goal. The HFWBM has been demonstrated to be capable of sustaining rates of 2400 b/s, 4800 b/s, 7200 b/s and 9600 b/s in 3 kHz channels. An innovation developed in this effort, a square-root Kalman equalizer adaptation algorithm, has been shown to have the tracking agility and stability characteristics required to successfully follow the time-varying HF channel. Designed with an integral automatic-repeat-request (ARQ) system, the HFWBM operating in this mode achieves very low error rate, high throughput, and is remarkably robust with respect to channel conditions. Notably, the error rate performance of the single tone HFWBM operating at 4800 b/s is significantly better than published results for multitone modems operating at 2400 b/s.

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1.0 EXECUTIVE SUMMARY

This Final Report has been prepared in complianc with CDRL Data Item A008 of RADC Contract No. F30602-79-C-0099 for an HF Wideband Modem (HFWBM). This contract is for an engineering effort to design, simulate, implement and test two HF modems capable of sustaining data rates of 4800 b/s or greater over standard 3 kHz HF channels. The Final Report incorporates an earlier Interim Technical Report covering the first twelve months of effort, which encompassed propagation analysis, modulation waveform parameter selection, overall modem and decision feedback equalizer (DFE) design, error control study, computer simulation, and real-time hardware and software design tasks. That material has been augmented with data describing the real-time modem implementation, preliminary (factory) acceptance testing and final (RADC DICEF) acceptance testing tasks. Results of an initial live link test have also been included here. Thus, the present report constitutes a complete summary of all technical work accomplished and information gained in performance of the contract.

A summary of significant accomplishments made over the complete contract effort is given in Table 1-1. Technical details underlying each accomplishment have been provided to the Sponsor through a series of monthly progress reports, technical memoranda, informal face-to-face briefings and formal oral presentations. Rather than repeat all of the minutiae contained in that material, only the significant results are summarized in the Interim and Final Reports. The content is carried to a sufficient depth to show how all of the contract technical requirements were met or exceeded in the successful completion of the effort. Frequent references are made to indicate where more details may be found in the auxiliary documents.

The main body of this report is organized into twelve major sections. Following this executive summary, Section 2 gives an overall description of the HF Wideband Modem and its expected operation. Section 3 summarizes the results of the analytical studies conducted in response to the requirements of paragraph 4.1 of the contract statement of work (SOW), which calls for "Study and assessement of High Frequency (HF) radio channel characteristics, adaptive equalization and bandwidth-efficient modulation/demodulation." Section 4 presents the results of computer simulations conducted in response to paragraph 4.2 of the SOW, which calls for "Development of a functional design and software algorithms for channel encoding, waveform modulation, and demodulation." Sections 5 through 8 discuss the real-time implementation of the final HFWBM algorithms on stand-alone programmable signal processors in accordance with paragraph 4.3 of the SOW. In particular, Section 5 deals with the hardware design and Section 6 describes the development of real-time software. Section 7 describes the support software made available for this effort from GTE independent development activities and special diagnostics written specifically for this application. Section 8 describes the actual HFWBM system development and identifies modifications made to the original design during the development and hardware/software integration phases. Sections 9 and 10 relate to the acceptance testing of the HFWBMs conducted in accordance with paragraph 4.4 of the SOW. Specifically, Section 9 documents the procedures used and results from the factory acceptance tests, while Section 10 does the same for the final acceptance tests conducted at RADC using the DICEF real-time channel simulator and a short live link. Section 11 summarizes the conclusions drawn from the successful completion of the contract and Section 12 presents our recommendations for future development and testing fo the HFWBM.

A separate technical report summary has been prepared to serve as a vehicle to rapidly convey the significant results to interested persons. This separate document has been made up from the material contained in Sections 1, 11 and 12 of the complete Final Report. Readers of the complete report may also find it useful to read these sections first as a quick overview of the program.

TABLE 1-1. SUMMARY OF ACCOMPLISHMENTS APRIL 1979 - NOVEMBER 1981

ANALYTICAL STUDIES (See Section 3)

- Developed statistical quantitative baseline for general HF channel perturbations for propagation distances up to 4000 nmi.
- Analyzed specific HF propagation predictions for transcontinental test link.
- Issued two technical memoranda documenting results of propagation analysis task [1,2]
- Derived M-ary PSK waveform modulation parameters in accordance with SOW criteria [3].
- Derived DFE receiver/demodulator design parameters for 2400 baud keying.
- Issued three technical memoranda documenting selected square-root Kalman DFE updating algorithm [4], jointly adaptive DFE and carrier recovery technique [5], and a data-derived synchronization algorithm [6].
- Assessed the quantitative trade-off between forward error correction (FEC) coding and the use of combined error detection and automatic request for retransmission (ARQ) [7].

COMPUTER SIMULATIONS (See Section 4)

- Developed functional design and software algorithms for channel encoding, modulation and demodulation.
- Utilized complete FORTRAN simulation software, including HF channel simulation algorithms developed under GTE independent development, to investigate modem behavior.
- Determined that the so-called "fast-Kalman" equalizer algorithm is numerically unstable.
- Explored other variants of Kalman estimation algorithms and found square-root formulation most suitable for fixed-point implementation.
- Utilized final modem design parameters in simulation to characterize error rate performance under a variety of simulated channel conditions.
- Prepared Program Maintenance Manual for all FORTRAN simulation software. [21]

REAL-TIME HARDWARE DESIGN (See Section 5)

- Surveyed array processor industry for an off-the-shelf machine capable of handling DFE processing for the HFWBM.
- Completed architectural definition and detailed logic design of a programmable high speed signal processor compatible with Mark IV processor and capable of performing DFE processing.
- Completed mechanical design and fabrication of HFWBM parts including KSP chassis and control panel and Mark IV control panel.

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TABLE 1-1. SUMMARY OF ACCOMPLISHMENTS APRIL 1979 - NOVEMBER 1981 (Cont.)

REAL-TIME SOFTWARE DESIGN (See Section 6) • Defined overall real-time software organization using structured high-level design techniques. • Designed, implemented and tested real-time Mark IV and KSP code on simulators. • Designed and implemented I/O software. • Prepared Program Maintenance Manual for real-time software [23].
SUPPORT SOFTWARE (See Section 7) • Designed and implemented a cross assembler for development of KSP micro code. • Developed KSP simulator and Mark IV application software diagnostics.
SYSTEM DEVELOPMENT AND INTEGRATION (See Section 8) • Modified standard Mark IV to provide 4 clock generators, KSP interface, 2-cycle multiplier, I/O drivers and audio AGC circuit. • Integrated real-time hardware and software and tested I/O functions. • Burned final software into Mark IV and KSP read-only memories.
FACTORY TESTING (See Section 9) • Prepared and successfully executed acceptance test procedure for nonfading channels [24]. • Demonstrated the HFWBM meets or exceeds all contract specifications.
DICEF TESTS (See Section 10) • Prepared and successfully executed acceptance test procedures for simulated fading channels [25]. • Compared performance on simulated channels with published results on multitone modems [26]. • Demonstrated successful operation on the air over a vertical incidence HF ionospheric link.

2.0 HFWBM DESCRIPTION

The HFWBM represents a new attempt to develop bandwidth-efficient, adaptive digital modems for HF radio communications. Bandwidth efficiency is commonly measured as the ratio of transmitted data rate in bits per second (b/s) to the spectral occupancy (measured according to some suitable criteria such as 90 percent energy) in Hertz. The fading dispersive nature of the HF channel has largely limited existing HF modems to efficiencies below 1.0 b/s/Hz. Existing and proposed requirements for greater communication reliability, lower error rates, and higher data rates now exceed this present operational capability.

The primary HF frequency allocations of initial interest are 3 kHz (SSB) channels commonly used for analog voice communications. Ultimately, there is interest in achieving the maximum possible signaling rates in 6 kHz (DSB) voice-bandwidth channels and possibly 10 kHz channels. The current HFWBM development is designed to provide selectable rates from 2400 b/s to 9600 b/s in 3 kHz channels (i.e., corresponding to spectral efficiencies from 0.8 to 3.2).

The HFWBM employs single carrier frequency (serial) M-ary PSK modulation at a 2400-baud signaling rate. This is in contrast with most of the present HF modems which use closely spaced parallel tones to achieve high ($\sim$0.8) spectral efficiency. To combat the effect of channel multipath, these present modems typically use a time guard band of 4-5 ms per symbol in which the receiver is effectively blanked. The HFWBM single-carrier, serial data

modulation technique offers the following advantages in relation to existing parallel tone modems:

a. It has a higher potential spectral efficiency

b. It uses all of the available post-detection signal-to-noise ratio (SNR)

c. It has a low ratio of peak-to-average signal power (thus peak power limited transmitters don't have to be derated as required for undistorted parallel tone operation)

d. It is less sensitive to frequency selective fading and narrowband co-channel interference

e. It is readily adapted to provide HF antijamming capabilities.

Against the above advantages is the fact that the high keying rate used with the HFWBM technique results in multipath-induced intersymbol interference (ISI) spread out over many symbols. The time varying nature of the HF channel requires more sophisticated adaptive processing techniques to undo the deleterious effects of ISI. The HFWBM capitalizes on two technological developments to overcome these difficulties; namely, the state-of-the-art has been advanced by:

a. Recent successful applications of Kalman filtering to adaptive equalization problems [4,8]

b. Large-scale integration (LSI), resulting in functional chips that are well suited to meet high-speed digital signal processing requirements.

The HFWBM uses a form of Kalman filtering to update the coefficients of an adaptive decision feedback equalizer (DFE). The Kalman coefficient updating algorithm has been shown to provide rapid start-up and fast adaptation to follow the time variations in the HF channel [9]. This has overcome the principal shortcoming (i.e., inadequate tracking agility) in previous attempts to effectively utilize wideband data signals over long-haul HF communication links. The particular form of the Kalman algorithm being used in the HFWBM, the square-root formulation, is well suited to implementation in a 16-bit fixed point processor.

The implementation of the processing functions in the HFWBM is split between software running in GTE Sylvania Systems Group Mark IV programmable signal processor and firmware associated with a high-speed peripheral processor developed by GTE under independent development. Generally, the Mark IV, which utilizes the AMD-2900 family of microprocessor devices, performs the lower rate and decision making functions (e.g., synchronization, carrier tracking, differential decoding, etc.). The high-speed operations associated with the equalizer adaptation are performed in the peripheral processor which utilizes four TRW MPY-16HJ multiplier chips in a parallel architecture. This combination of processors can handle the worst-case computational load corresponding to a T/2-spaced DFE designed for 5 ms multipath spread at 2400 baud.

The HFWBM combines adaptive equalization and ARQ techniques for effective error control on severely fading channels. The ARQ technique is based on a continuous GO BACK N scheme modified to include a short burst of equalizer training data at the start of each group of N repeated transmissions. The ARQ feature may be disabled and training introduced on a fixed (selectable) duty

cycle. This disabling can remove the necessity for the return link on moderately fading channels.

Figure 2-1 shows the HFWBM front panel that interfaces to the Mark IV programmable signal processor. Table 2-1 gives a brief description of each of the controls and indicators. Figures 2-2 and 2-3 show overall functional block diagrams of the modulator and demodulator processing, respectively. The technical details of the algorithm designs are described in Section 3 and in references [1-7] previously supplied to the sponsor.

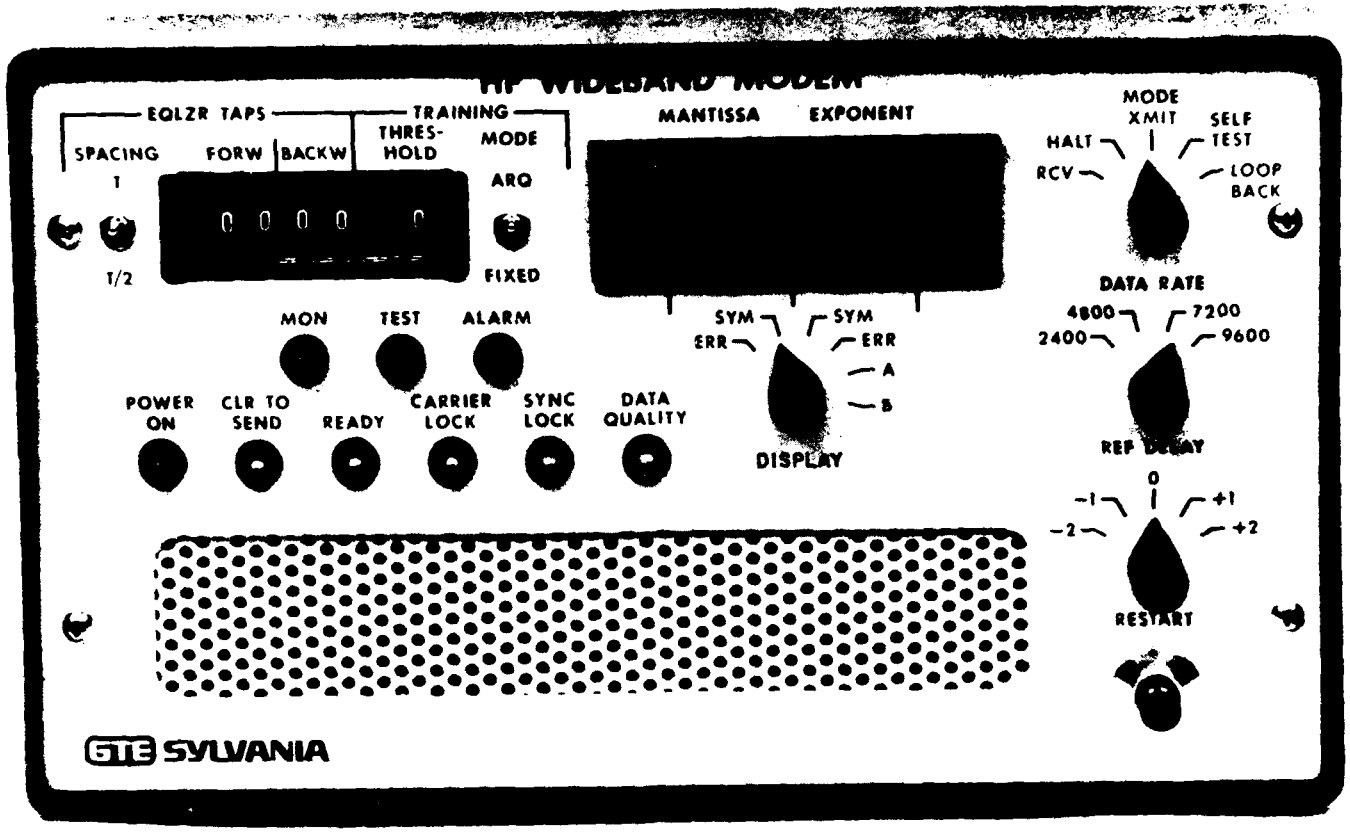

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Figure 2-1. HFWBM Front Panel

TABLE 2-1

HFWBM CONTROLS AND INDICATORS

LABEL	TYPE*	USE
SPACING	TSW	Selects between T and T/2 tap spacing in the feed-forward equalizer
FORW	THSW	Sets number of feed-forward equalizer taps
BACKW	THSW	Sets number of feedback equalizer taps
THRES-HOLD	THSW	Sets SNR threshold for ARQ (TRAINING MODE=ARQ), or sets duty cycle for periodic training (TRAINING MODE=FIXED)
MANTISSA	LED	Displays two-digit mantissa of selected display value
EXPONENT	LED	Displays sign and two-digit exponent of selected display value
MODE	RSW	Selects between receive (RCV), halt, transmit (XMIT), self-test and loop-back modes
MON	PL	Spare monitor light
TEST	PL	Indicates modem is in self-test or loop-back mode
ALARM	PL	Indicates PASS/FAIL test result
POWER ON	PL	Indicates power ON/OFF
CLR TO SEND	PL	Indicates clear to send status when in XMIT mode
READY	PL	Indicates data set ready status when in XMIT mode
CARRIER LOCK	PL	Indicates carrier lock when in RCV mode
SYNC LOCK	PL	Indicates synchronizer lock when in RCV mode
DATA QUALITY	PL	Indicates data quality status when in RCV mode

TABLE 2-1 (continued)

HFWBM CONTROLS AND INDICATORS

LABEL	TYPE*	USE
DISPLAY	RSW	Selects display value: total error count (TOTAL ERR), total symbol count (TOTAL SYM), data symbol count (DATA SYM), data error count (DATA ERR)
DATA RATE	RSW	Selects among 2400, 4800, 7200 & 9600 b/s data rates
REF DELAY	RSW	Shifts synchronization of local reference (training) pattern
RESTART	PB	Causes modem to start at the beginning of the program associated with the selected MODE

*TSW - Toggle switch
THSW - Thumbwheel switch
LED - Light emitting diode digital readout
RSW - Rotary switch
PL - Pilot light
PB - Push button

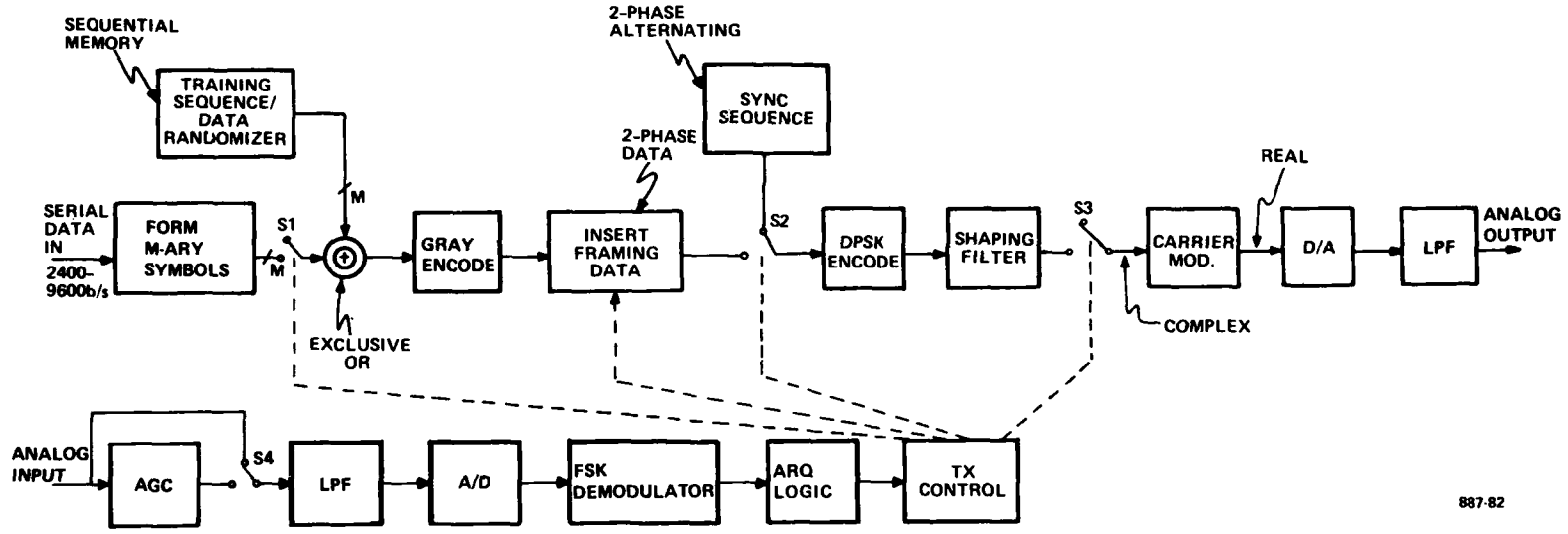

Figure 2-2. Overall Block Diagram of PSK Modulator/ARQ Receiver

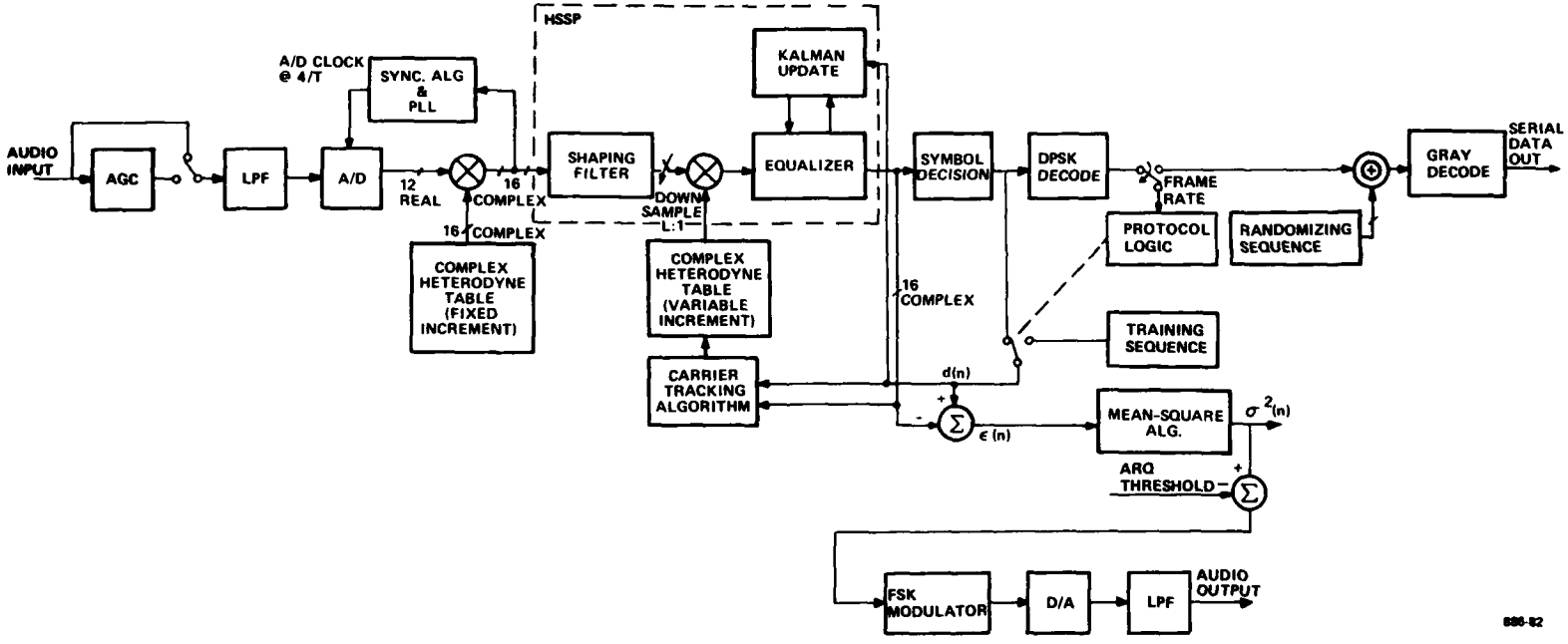

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Figure 2-3. Overall Block Diagram of PSK Demodulator/ARQ Modulator

3.0 ANALYTICAL STUDY RESULTS

The objectives of the analytical study effort were to:

a. Assess HF radio channel characteristics and establish a statistical quantitative baseline for HF channel perturbations (fading rates, fading depths, frequency selectivity, multipath spread)

b. Derive waveform modulation parameters in accordance with criteria specified in the SOW

c. Derive DFE receiver/demodulator design parameters compatible with the selected modulation

d. Assess the quantitative trade-off between forward error correction coding and the use of combined error detection, ARQ, and retransmission.

The results in each of these areas are summarized in the four subsections which follow. Further details may be found in references [1-7] previously supplied.

3.1 Propagation Analysis

A global bank of data does not exist from which the system planner can accurately estimate the variation of HF fading perturbation parameters with location, season, time-of-day, sunspot number, frequency, path length, etc. What is available consists of greatly simplified theoretical models and a small number of reports by experimentalists involving a limited portion of the range covered by these variables. Thus, baseline estimates of the perturbation parameters are possible only insofar as they can be reasonably supported

by simplified models and experimental data for conditions not too different from the actual links to be utilized. For the present effort, this generally means propagation distances up to 4,000 nmi in the temperate latitudes.

The results contained in [1] can be summarized as follows. Because of an apparently large statistical variation of fading speed with frequency, the investigation of fading rate concluded with different estimates for different frequency ranges. Defining f_e as the average rate of excursions of the received envelope downward across its mean value, the suggested estimates are:

Frequency	f_e
6-7 MHz	.31 Hz
8-14	.18
15-18	.12

The fading rate at any other level r is given by

$$f(r) = 2rf_e \exp(-0.693r^2)$$

where r is the ratio of that level to the median envelope. This is based on a Rayleigh scattering model. The Rayleigh model allows for fade depths down to zero signal level, albeit with vanishingly small probability. The probability of a fade to depth r is given by

$$P(r) = 1 - \exp(-0.693r^2)$$

The mean duration of fades at level r is

$$\bar{t} = P(r)/f(r)$$

Table 3-1 lists various relative fade depths, their probability of occurrence and their normalized duration, $f_e\bar{t}$. It should be noted that the Rayleigh scattering model does not account for discrete Doppler-shifted multipath components which can combine at the receiver to cause more rapid frequency-selective fades to slide through the spectrum. In this case, the fade rate is determined by the total Doppler spread, and the average fade duration is given approximately by the reciprocal of the Doppler spread. The depth of this type of fading is given by the difference between the received levels of the individual multipath components. In the HFWBM application, the DFE acts to coherently combine the individual multipath components in a kind of "implicit diversity," so the multipath-induced fading is not an important issue.

The degree of frequency selectivity in the fading signal is determined by the total multipath spread. Stated another way, the range of frequencies that undergo a similar (flat) fading process is known as the coherence bandwidth B_c, which is given approximately by the reciprocal of the multipath spread. Again, frequency selective fading can be a significant problem in parallel tone modems (without coding), but is not a crucial issue for the HFWBM. What is crucial to the HFWBM is the underlying total multipath spread. For this reason (and since B_c can be computed from the multipath spread), the study focused on multipath.

Typically, multipath spread is a function of both frequency and path distance. The Institute for Telecommunications Sciences (ITS) has constructed useful multipath curves displaying multipath spread trends from experimental data encompassing a wide range of paths and frequencies. Table 3-2 shows data taken from these curves for a 4,000 nmi path. Working as close as possible to the maximum usable frequency (MUF) tends to minimize multipath spread for all

TABLE 3-1. FADE DEPTH, PROBABILITY OF OCCURRENCE AND NORMALIZED DURATION

r(dB)	P(r)	$f_e\bar{t}$
0	.5	.5
- 5	.2	.2
-10	.07	.1
-20	.007	.03
-40	.00007	.003

TABLE 3-2. MULTIPATH SPREAD FOR 4,000 NMI HF LINK

Operating Frequency	Spread
100% of MUF	<0.5 ms
88% of MUF	0.5 ms
75% of MUF	1.0 ms
60% of MUF	2.0 ms
<60% of MUF	>2.0 ms
Maximum Expected	3.2 ms

distances. The maximum multipath spread at low frequencs increases for both short and long path lengths. At 540 nmi, the maximum expected multipath spread is about 5 ms.

Extensive propagation predictions were made for a planned on-the-air HF test link between GTE West in Mountain View, California, and RADC in Rome, New York.* The prediction data were obtained using a computer program (HFMUFES-IV) available from ITS. Table 3-3 lists the input data to the program. Method 7 causes data to be tabulated for all modes. The frequency range of 12-22 MHz was determined to encompass the "optimum working frequency" (FOT), in an initial pass through the HFMUFES-IV program. The combination of transmitter power and antenna characteristics were arbitrarily chosen to establish a baseline from which the performance of other alternative configurations could be easily predicted. The level of man-made noise at the receive site, -148.6 dBW, corresponds to the standard category of "suburban" man-made noise. Other standard categories are "urban" (-136.5 dBW) and "rural" (-165.6 dBW). The month of June, 1980, was chosen to reflect the seasonal extreme closest to the expected test period. A relatively high sunspot number (180) was used to reflect the anticipated abnormally high level of solar activity during this expected test period.

Analysis of the prediction data focused on the multipath data and their relationships to relative signal power and choice of operating frequency. Detailed results are given in [2]; the conclusions drawn are summarized in Table 3-4.

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*At the end of the HFWBM study phase, a decision was made by the Sponsor to delete the live link tests from the current contract. The material in the rest of this section is included simply for completeness to document activities undertaken during the study phase for possible use at a later date.

TABLE 3-3. INPUT DATA FOR PROPAGATION PREDICTIONS

Method	7
Time of Day (in 1-hour increments)	0100-2400
Frequency (in 2-MHz increments)	12-22 MHz
Min. take-off angle	0.
Transmitter power	5.0 kW
Required SNR (in 1 Hz bandwidth)	40 dB
Man-made noise at receive site	-148.6 dBW
Required reliability	90%
Transmit and receive antennas:	
Type	Horizontal Dipole
Height	$\lambda/4$
Length	$\lambda/2$
Orientation	N-S
Conductivity	.01
Dielectric constant	16
Frequency range	12-22 MHz
Month, year	June, 1980
Sunspot number	180

TABLE 3-4. SUMMARY OF CONCLUSIONS DRAWN FROM PROPAGATION PREDICTIONS

- The principal propagation mode for the test link will be 2F.
- The test link will have 3 or fewer multipath components over 90% of the time.
- Nearly half of the time, the strongest component will not be the first to arrive.
- The maximum multipath spread may be regarded as 4.9 ms.
- Over 90% of the time, the multipath spread will be 4.0 ms. or less at all frequencies from 12 MHz to 22 MHz.
- Use of frequencies near the FOT will result in multipath spreads that are less than 3.0 ms. more than 95% of the time.
- Use of high gain antennas, or transmitter power greater than 5 KW may be required to guarantee 10^{-3} symbol error rate (without error control) at 4800 b/s at all hours of the day.
- 10^{-3} symbol error rate at 7200 b/s is at least theoretically achievable with a 5 KW transmitter and half-wave dipole antennas during some nighttime hours.
- Choosing a time/frequency plan to maximize predicted service probability represents an effective way to optimize the chances for success of the test link.

Subsequent to completion of the propagation analysis task, site visits to suggested transmit and receive locations near RADC were undertaken, and further details on GTE West facilities were obtainend. The transmitter equipment at the Ava, New York, site appears ideally suited for the main high data rate forward link. This equipment includes Collins 310-F1 exciters, Collins 208-U3 (3 kW) and 208-U10 (20 kW) transmitters, Collins 237-A1 and 237-B1 log periodic antennas and other general-purpose HF receivers and antennas. A key feature of the transmitting equipment for use with the HFWBM is the ability to phase lock the carrier to a cesium beam frequency standard at the site. This will provide a very stable RF for the M-ary PSK modem. Table 3-5 lists the frequency allocations available at Ava for use with 3 kHz audio bandwidth data modems.

The Forrestport, N.Y., site is a newly refurbished VLF experimental station that could be used as either the primary or return link receive site. It has no applicable HF equipment at present, however, a~80' microwave tower is in place that could support a log-periodic antenna. The primary advantage of Forrestport is its remote location on a plateau at the edge of the Adirondack Mountains, where ground conductivity is reported to be good and man-made electrical noise low. No quantitative data on the HF background noise level was available; such data would be of considerable interest to see if the "rural" categorization (17 dB improvement over "suburban") is more appropriate.

The facilities at Mountain View, CA, consist of two steel antenna towers, each ~ 50 feet high, 60 feet apart in a N-S line. Each tower has an equipment cabin 12'x12'x8' interior with a deck and railing on top. One tower is loaded with transmitters and VHF/UHF antennas on top. The other which was formerly a receiver tower is empty. Again, no data is available on ambient electrical

TABLE 3-5. RADC HF FREQUENCY ALLOCATIONS FOR AVA, N.Y.

kHz
3081
5688
8967
11214
13211
15048
18023
20860
23885
26529
27920

noise levels at HF. Taking such measurements would be of interest since there is concern that the test link would be looking across the edge of San Jose.

3.2 Waveform Design

It is well known that pulse amplitude modulation (PAM), phase shift keying (PSK) and combined PAM/PSK constitute bandwidth-efficient modulation techniques. Although combined PAM/PSK constellations are more optimum from an error-rate point of view for large alphabets, the difference between 8-ary PSK and the optimum 8-ary constellation is only about 1.8 dB, and the difference between 16-ary PSK and the optimum 16-ary constellation is about 4.1 dB. Binary and 4-ary PSK represent optimum signal sets. Besides being simpler to implement, M-ary PSK is relatively insensitive to amplitude fluctuations that are present on a fading channel. Thus, single carrier M-ary PSK modulation (with M=2, 4, 8 or 16) has been selected for the HFWBM because:

- It satisfies the single carrier requirement (SOW paragraph 4.1.2.1)
- It satisfies the peak-to-average modulated signal envelope constraint (SOW 4.1.2.2)
- It has a high bandwidth efficiency, i.e., it allows high data rates in given spectral occupancies, (SOW 4.1.2.3)
- It is relatively easy to provide for different data rates by using M-bits per baud encoding at a fixed symbol rate (SOW 4.1.2.5)
- The error rate for M-ary PSK compares favorably with hybrid PSK/PAM modulations (see [10])

- It is less vulnerable to the amplitude variations that will be present on an HF fading channel.

Having selected M-ary PSK modulation, there remains the choice of keying rate and pulse shaping parameters. The rationale for selecting 2400 baud keying and 50 percent roll-off square-root raised cosine spectral shaping is documented in [3]. Briefly, these selections:

- Provide the capability for data rates of 2400, 4800, 7200 and 9600 b/s (SOW 4.1.2.6)*
- Have nonpositive cross correlation of time adjacent symbols (SOW 4.1.2.4)
- Provide an envelope peak-to-average ratio of 1.1 dB (SOW 4.1.2.2 requirement is < 3 dB)
- Have been shown (see Section 4.2) to have a symbol error rate versus noise characteristic within 1.5 dB of that for ideal PSK in white Gaussian noise (SOW 4.1.2.7).

*Only 2400 b/s and 4800 b/s are strict requirements of the SOW. The 9600 b/s rate is a stated goal; the 7200 b/s rate is an easily added feature (uses 8-ary PSK at 2400 baud) that has proven workable in fading channel computer simulations.

The square-root raised cosine spectral shaping is implemented in a 19-tap finite impulse reponse (FIR) filter operating at a nominal 7200 Hz sample rate**. The choice of a 50 percent roll-off for the raised-cosine characteristic results in a 99 percent signal energy spectral occupancy of 3 kHz for the actual FIR filter. The response of the FIR filter is shown in Figure 3-1. It was shown that implementation of this filter in 16-bit fixed point arithmetic was essentially equivalent to infinite precision.

3.3 Modem/DFE Design

Once the modulation waveform parameters were selected, the adaptive DFE receiver/demodulator functional design was developed. Key issues that were investigated included the DFE adaptation algorithm, functional spacing of the feedforward filter, carrier recovery, and symbol synchronization. The results of these studies are summarized below.

3.3.1 Adaptive Equalizer Algorithms

The most crucial issue by far was the design and verification of adaptive equalization algorithms and techniques capable of tracking variations in the HF channel disturbances. The desired characteristics of the equalizer included:

- Sufficient acquisition and tracking ability to accommodate fade rates up to 1 Hz (SOW 4.1.3.1),
- Operation with channel multipath spread up to 5 ms (SOW 4.1.3.2),

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**"Nominal" is used here to indicate design rates in the absence of any time compression to support ARQ overhead. Actual rates will be 4 percent higher when this overhead is included.

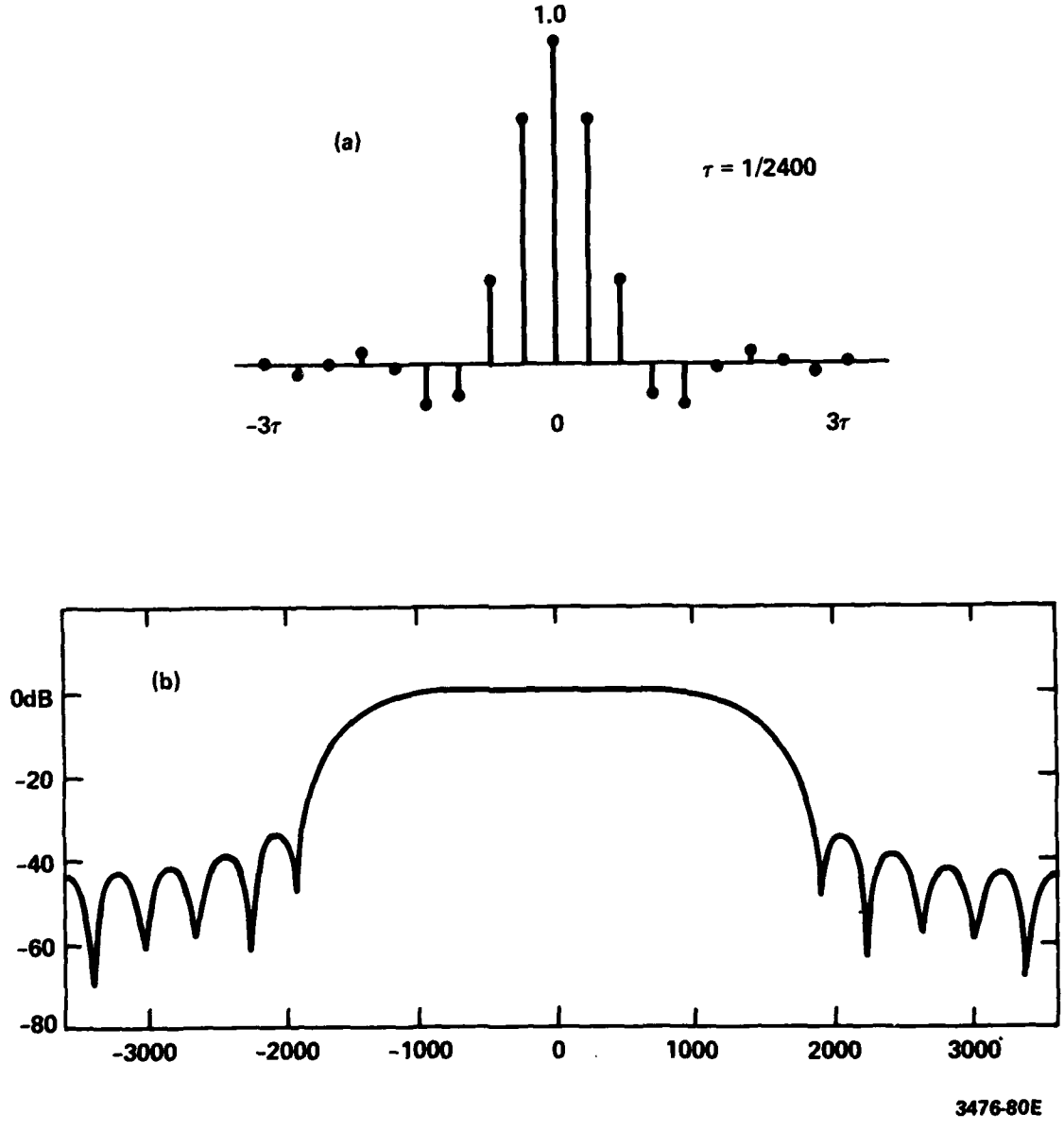

Figure 3-1. Response of FIR Pulse Shaping Filter:
(a) Unit Sample Response, (b) Frequency Response

- Equalized symbol error rate performance within 8 dB of theoretical for fade rates up to 2 Hz and multipath spreads up to 5 ms (SOW 4.1.3.3),
- High computational efficiency (low processor burden), and
- Insensitivity to computer round-off errors (numerical stability).

Linear equalization was not considered because of its inability to handle spectral nulls common in HF frequency selective fading. It is well known that a decision feedback equalizer (DFE), such as shown in Figure 3-2, does not suffer from this limitation.

By the time the proposal for the HFWBM was written, GTE indepdendent research and development studies had already shown that a DFE using the traditional "steepest descent" tap adjustment algorithm could not track the rapidly varying HF channel. Those same studies had successfully applied a form of Kalman filter to solve the channel tracking problem. Specifically, floating point computer simulations had demonstrated the ability of a DFE to successfully track a two-path fading channel using what will be referred here to as the "conventional Kalman" tap weight adjustment algorithm. At about the same time, Falconer and Ljung published a "fast Kalman" algorithm [11] which was reported to be equivalent to the conventional algorithm but required far fewer operations per iteration (proportional to the number of equalizer taps, rather than the square of the number of equalizer taps). Figure 3-3 shows the relative processing burdens, as measured by the number of multiplications per iteration, for the conventional Kalman, fast Kalman and steepest descent (gradient) methods. The computational burden of the fast Kalman method depends additionally on whether the feedforward equalizer is operated with

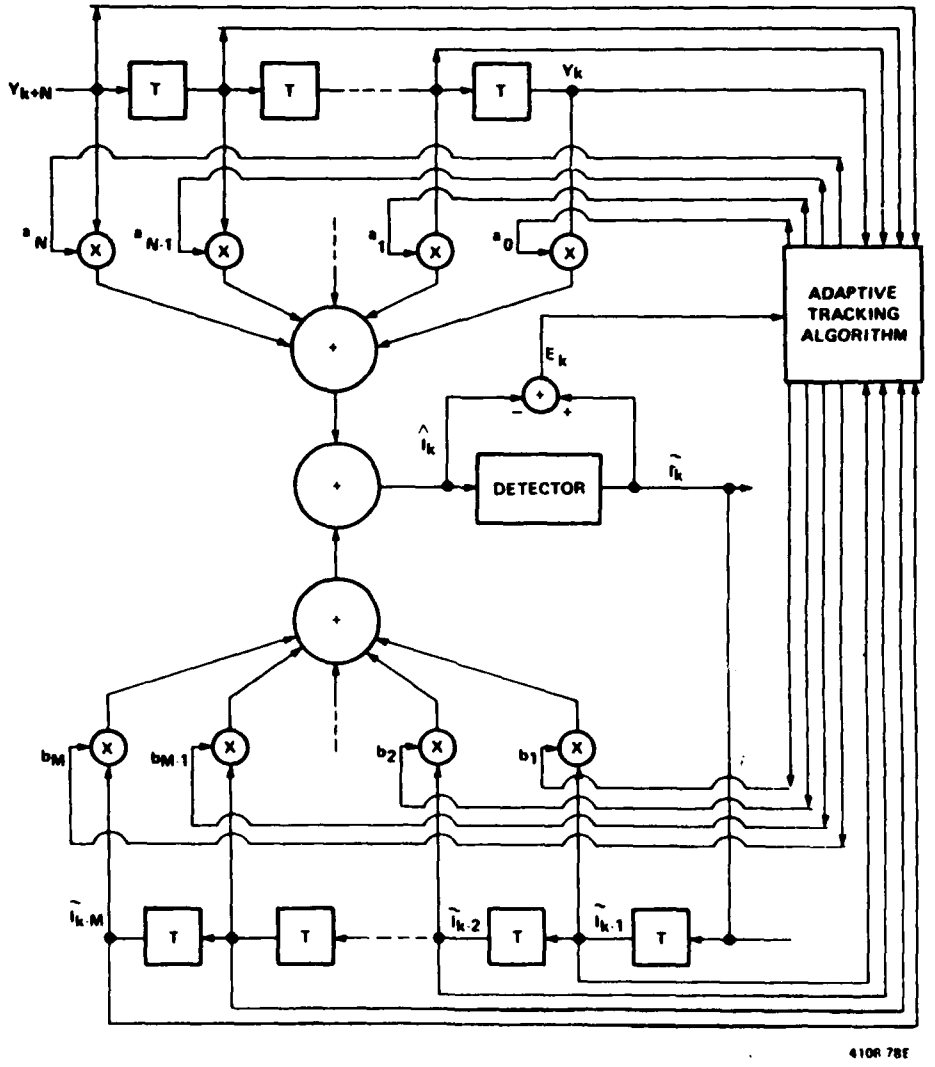

Figure 3-2. Decision Feedback Equalizer for T-Second Spacing

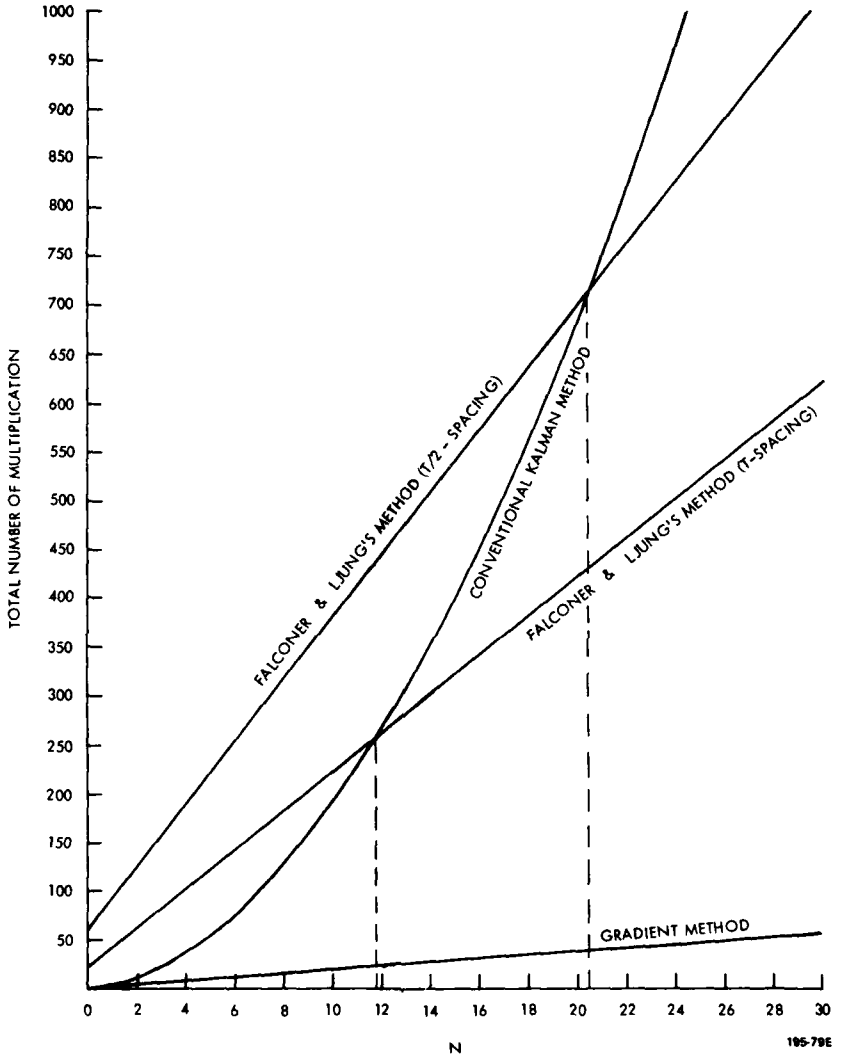

Figure 3-3. Processing Burdens for Various Equalizer Adaptation Algorithms

symbol spaced (T) or fractionally spaced (e.g., T/2) samples. For a T/2-spaced DFE, the fast Kalman algorithm appears to be computationally more efficient than the conventional algorithm whenever the total number of taps exceeds 21. For a T-spaced DFE the cross-over is around 12 total taps.

Considerable effort was spent in exploring ways to apply Falconer and Ljung's fast Kalman algorithm to the time varying channel. All of the investigations led to the same result: the fast Kalman algorithm is unstable for the time-varying channel. Consultation with members of the Technical Staff at Bell Telephone Laboratories confirmed instabilities associated with the fast Kalman algorithm; they had in fact noted high sensitivity to computer round-off errors. This coupled with our own negative experiences in implementing even the conventional Kalman algorithm in 16-bit fixed point arithmetic eventually led us to the selection of a square-root formulation of the Kalman algorithm.

The "square-root" Kalman algorithm effectively involves the computation of the Kalman error covariance matrix in factored form: the so-called $U\text{-}D\text{-}U^T$ decomposition described by Bierman and others [12-20]. U is an upper triangular matrix and D is a diagonal matrix. The improved numerical behavior of this method is due in large part to a halving of the dynamic range required to represent the elements of U. Judicisious scaling thus allows the square-root algorithms to achieve accuracies that are comparable to a conventional Kalman algorithm that uses twice the numerical precision.

The details of the square-root formulation of the Kalman equalizer adaptation algorithm have been derived in [4], which has been previously supplied. Table 3-6 shows the computational burden of this algorithm. Note that despite its name, this form of the algorithm does not require any

TABLE 3-6. COMPUTATIONAL REQUIREMENTS PER SQUARE ROOT KALMAN ALGORITHM

Operation	Complex Multiplies	Half Complex Multiplies	Real Multiplies	Real Reciprocals	Complex Adds	Real Adds	Total Equivalent	
							Real Mults.	Real Adds
3.1 Calculate Error	N				N		4N	4N
3.2 Calculate F_N	N(N-1)/2				N(N-1)/2		$2N^2-2N$	$2N^2-2N$
3.3 Calculate V_N		N					2N	
3.4 Calculate ϕ_{N+1}			2N			2N	2N	4N
3.5 Calculate ϕ_{N+2}			1			N+1	1	N+1
3.6 Calculate Υ_{N+1}				N+1			6N+6	5N+5
3.7 Update Δ_{NN}			N				N	
3.8 Calculate K_N	N(N-1)/2				N(N-1)/2		$2N^2-2N$	$2N^2-2N$
3.9 Calculate W_N		N-1					2N-2	
3.10 Update U_{NN}	N(N-1)/2				N(N-1)/2		$2N^2-2N$	$2N^2-2N$
3.11 Calculate Γ_N			N				N	
3.12 Update Δ_{NN}			N				N	
3.13 Update C_N	N	1			N		4N+2	4N
TOTAL	$\frac{3}{2}N^2+\frac{1}{2}N$	2N	5N+1	N+1	$\frac{3}{2}N^2+\frac{1}{2}N$	3N+1	$6N^2+17N+7$	$6N^2+12N+6$

square-root operations. The total multiply rate is nearly identical to the conventional Kalman algorithm.

As suggested in [4], it has been found useful to periodically reset the U-D factors to represent a diagonal matrix. This further stabilizes the numerical behavior of the algorithm in fixed-point implementations, and has little adverse effect on error rate performance. The HFWBM performs this resetting at the frame rate (every 100 symbols).

3.3.2 Carrier Recovery

A jointly adaptive DFE and carrier recovery technique was developed for the HFWBM. This technique allows the receiver/demodulator to extract carrier tracking information directly from the data signal thus eliminating the need to transmit special pilot tones. Figure 3-4 shows a functional block diagram of the algorithm. The adjustment of the equalizer tap coefficients and of the estimate of the current channel phase shift is based on Kalman and second-order phase-locked loop (PLL) filters respectively for jointly minimizing the squared-error with respect to those parameters. Analysis and simulation results presented in [5] demonstrate that this technique achieves excellent performance for rapidly fading channels with high frequency offset and phase jitter conditions.

3.3.3 Symbol Synchronization

A data-derived symbol synchronization technique was designed for the HFWBM. The algorithm operates on the passband input and is therefore decoupled from the jointly adaptive carrier recovery and DFE loops. A functional block diagram of the symbol sync algorithm is shown in Figure 3-5. Since the received data does not contain a line component at the keying rate,

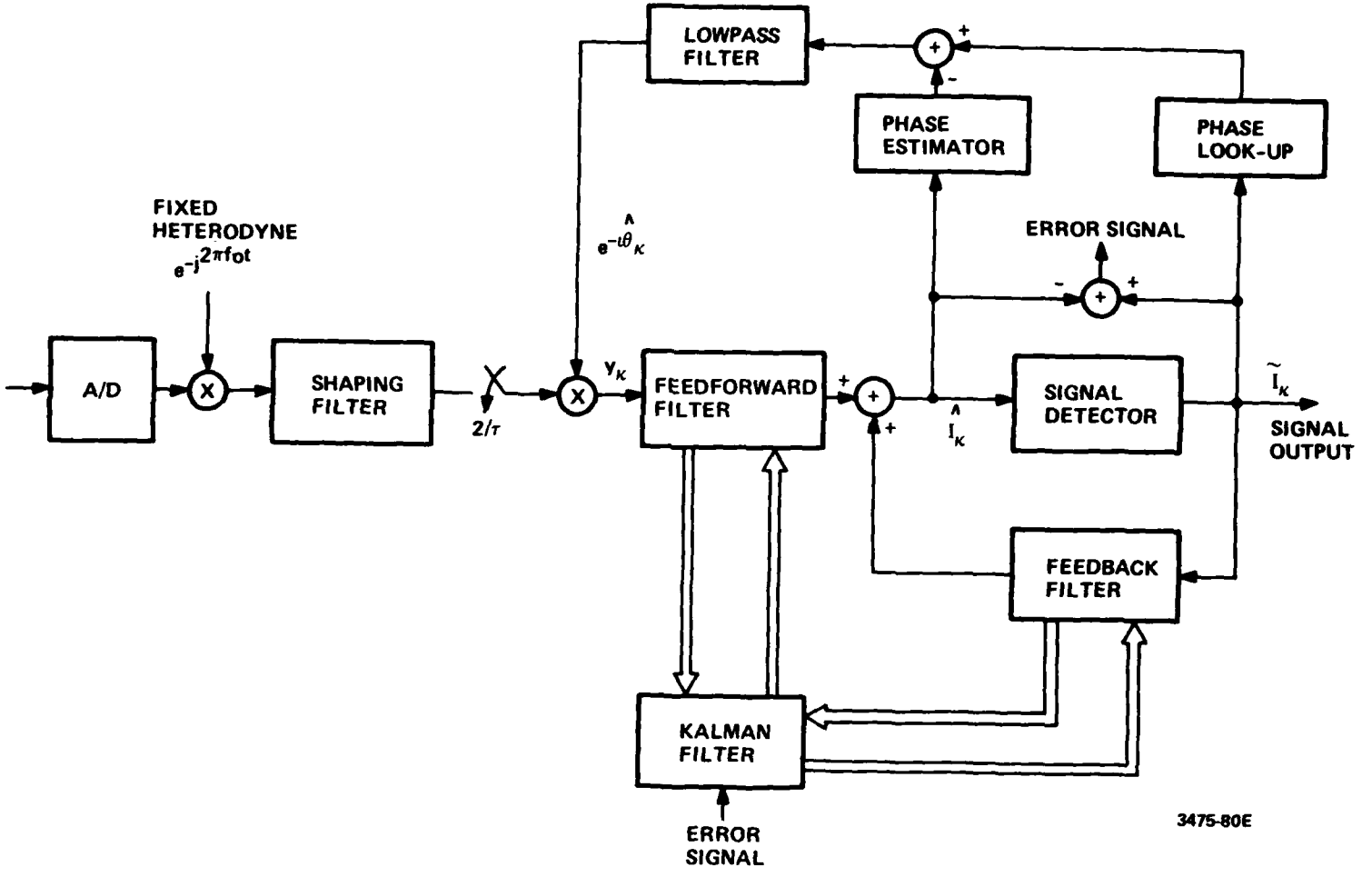

Figure 3-4. Functional Block Diagram of Carrier Tracking Algorithm

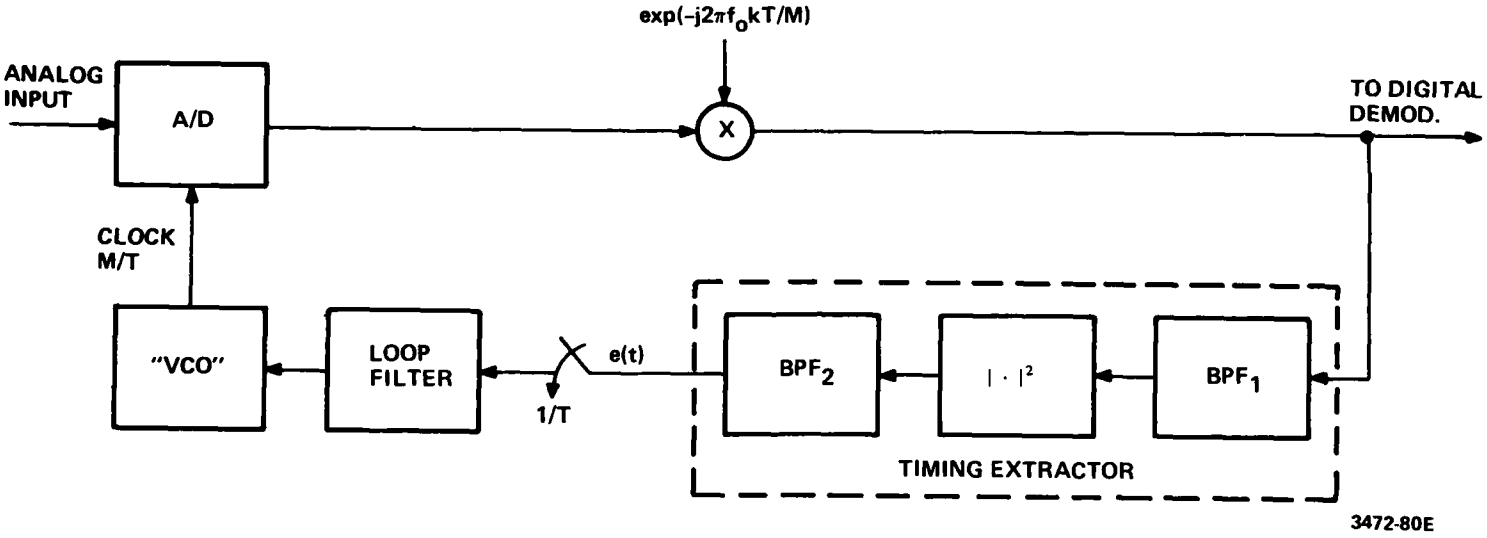

Figure 3-5. Functional Block Diagram of Symbol Synchronization Algorithm

the generation of a symbol clock requires some form of nonlinear processing on the received data. The analysis given in [6] shows how envelope or square-law detection of suitably filtered incoming data provides the desired component at the keying rate. A second-order PLL is used to acquire and track this rate so that A/D samples may be taken at some multiple (the HFWBM uses 4 samples per symbol, or a nominal 9600 Hz sample rate). Computer simulations have shown that with suitably chosen filters, this technique is quite robust with respect to frequency offset and intersymbol interference.

3.3.4 Acquisition Process

Before transmitting any data, the HFWBM cycles through an initial acquisition procedure to establish time and carrier synchronization. Under normal conditions this procedure is executed only once; however, it can be reentered through either a manual or system RESTART command. The first ten frames of the acquisition process consist of pure carrier to permit the demodulator to make an initial estimate of carrier frequency. The next ten frames consist of alternating data to allow for an estimate of baud rate. Two hundred forty frames of data alternated at the frame rate allows synchronization in the demodulator between the data stream and the local training sequence generator. The last four frames of transmitted acquisition data train the equalizer. A flow chart for the modulator acquisition process is shown in Figure 3-6.

During acquisition the demodulator first waits in a loop for a detector to recognize the presence of pure carrier. After the detector indicates the end of pure carrier, the correction increment generated by the carrier PLL is moved from the second heterodyne to the first. This is done to allow the symbol synchronizer to operate on a signal reasonably close to baseband.

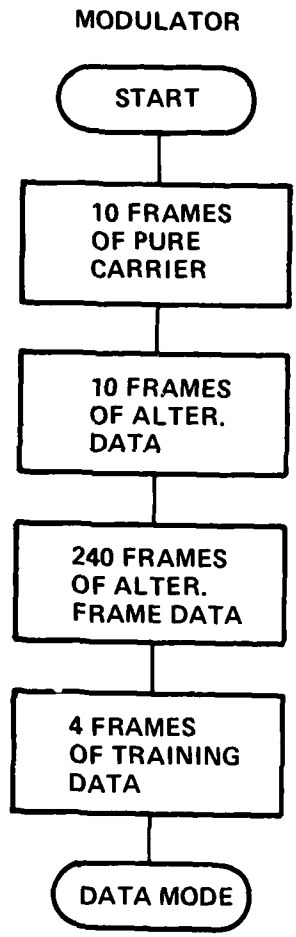

Figure 3-6. Flow Chart for Modulator Acquisition Process

Normally, the alternating data detector will turn on and the symbol synchronizer will converge on a correct strobe rate for the A/D convertter. At the end of this period, the bandwidth of the sync PLL is reduced by a factor of 10 for operation in the steady state mode. At this point, both the carrier and synchronizer PLLs are turned off. The frame sync process averages over frames of alternating data that have been quadrature-demodulated. The result is used to determine the time of the first arriving multipath component in a frame. At the end of this period, all systems can be turned on and the equalizer is trained. If there were no time-outs during the entire algorithm, the HFWBM would be in the final data mode. Any loop time-out condition leads to generation of a system RESTART command. Figure 3-7 shows a flow chart of the demodulator acquisition process.

3.4 Error Control Trade-Off Study

A study was conducted to assess the quantitative trade-off between forward error correction (FEC) coding and the use of combined error detection, ARQ, and retransmission. The results given in [7] show that for fading HF links, ARQ is generally superior to FEC in both throughput rate and undetected error rate. A continuous GO BACK 3 ARQ system was shown to be a good choice for propagation distances up to 4,000 nmi. Considerations of throughput efficiency and equalizer training delay led to the selection of 100-symbol data frames. A return link data rate of 300 baud was suggested.

The proposed ARQ system fits naturally and easily with an automatic request for training (ART) scheme for the adaptive equalizer. Because the equalizer needs retraining only during or after signal fades, ART has been found much more effective, again in terms of both error rate and throughput, than fixed percentage periodic training. The combined ART/ARQ operation of

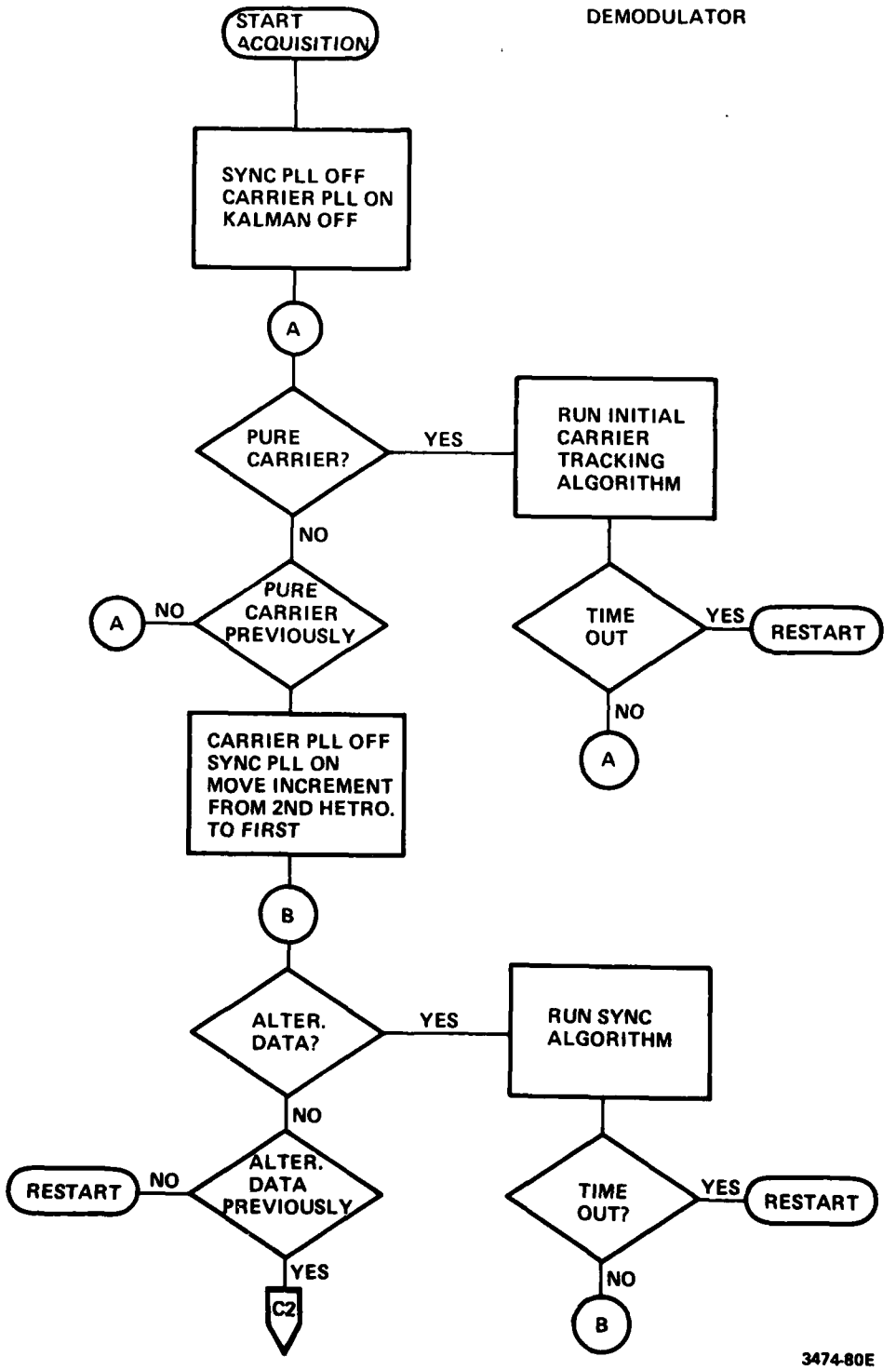

Figure 3-7. Flow Chart for Demodulator Acquisition Process (Sheet 1 of 2)

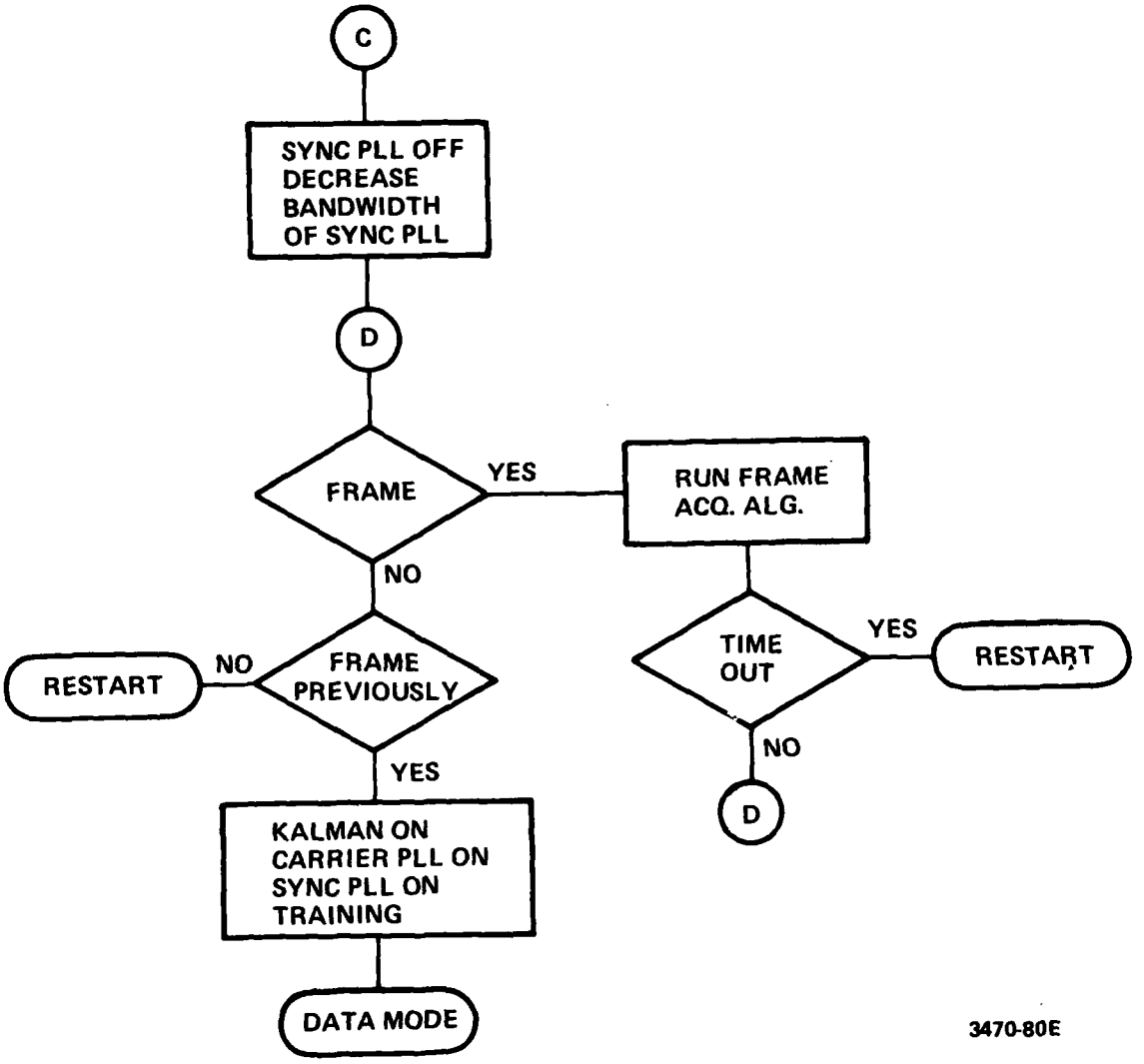

Figure 3-7. Flow Chart for Demodulator Acquisition Process (Sheet 2 of 2)

the HFWBM proceeds as follows. The mean-square-error (MSE) in the equalizer output is continuously monitored and compared to a threshold. Whenever the MSE rises above a preset threshold, an ART/ARQ message is sent via a return link back to the data transmitter. Beginning with the first frame following detection of this message, the data modulator transmitter switches to the ART/ARQ mode. In this mode, the modulator/transmitter first sends one frame (100 symbols) of the known equalizer training sequence followed by a repeat of the previous three data frames. At the end of this (4-frame) period, the modulator/transmitter either returns to the normal data mode (if the return link is clear), or remains in the ART/ARQ mode (if the return link continues to carry the ART/ARQ message). More than 256 ART/ARQ messages in succession cause the HFWBM to go back into a complete reacquisition.

An analysis of how to set the ART/ARQ threshold showed that one corresponding to a 6 dB instantaneous SNR is a good compromise to cover a wide range of HF fading conditions. Table 3-7 illustrates the performance expected when using this threshold. Bit-error-rates (BER) are given for binary DPSK received over either a flat Rayleigh fading or two-component multipath fading channel with 20 dB mean SNR. The throughput efficiencies achieved with the ARQ system are higher than the code rates that would be required for a (127, k) BCH FEC block code to achieve the same error rate reduction. Comparisons with FEC assume that FEC is used with sufficient interleaving to effectively randomize all burst error patterns. Such interleaving would necessitate substantial buffering and introduce long delays for high speed serial data transmission over fading HF links.

TABLE 3-7. PREDICTED PERFORMANCE OF RECOMMENDED GO BACK 3 ARQ TECHNIQUE

	Flat Rayleigh Fading	Two Component Multipath Fading
BER (Before ARQ)	5.0×10^{-3}	4.9×10^{-5}
BER (After ARQ)	8.9×10^{-5}	4.4×10^{-6}
Throughput Efficiency	.86	.997

TABLE 3-8. CHARACTERISTICS OF RECOMMENDED ARQ SYSTEM

Parameter	Value
Block size	100 symbols
No. repeated blocks	3
Equalizer training	100 symbols
Return link data rate	300 baud
Max. equalizer training delay	120 ms.
Protocol overhead	4%

The error control trade-off study included the effects of errors in the return link of the ARQ system. It was shown that, in a practical system, it should be relatively easy to maintain greater than 90 percent forward throughput efficiency even when these errors are included. Table 3-8 summarizes the salient characteristics of the recommended ARQ error control system.

4.0 SIMULATION RESULTS

4.1 Overview of Computer Simulation

The FORTRAN simulation consists of four major components: PSKMOD, CHANSM, PSKDMD and DEMSTR. Each component is designed to run as a standalone program. The interrelationships of these components is shown in Figure 4-1.

PSKMOD simulates the analog output of an M-ary (2, 4, 8 or 16) PSK modulator. The significant digital processing operations of the modulator are simulated using fixed precision arithmetic. The analog bandpass filter in the transmitter is represented by either a seventh order elliptical filter or a linear FIR filter. The modulator generates both an initial acqusition sequence and a steady state data mode. Since the modulator must run in a stand-alone mode, ARQ is not simulated. The analog output of the modulator is written as a binary data file.

CHANSM simulates a Rayleigh (or Rician) fading multipath channel with additive Gaussian and atmospheric noise. There are four complex paths with individually selectable tap gains, specular components and Doppler shifts. Each tap has an adjustable delay of 0-127 samples. Taps may be used either as C.W. interferors or multipath tap weights. The tap gains are computed as the outputs from second-order Butterworth filters driven by independent complex-valued Gaussian random processes. The fading rate is controlled by the filter bandwidths. The binary data output file from the modulator serves as the input file to the channel simulator. Either the complex data can be used directly or the imaginary part can be ignored and recreated through a Hilbert transform. Figure 4-2 shows a block diagram of the channel simulator.

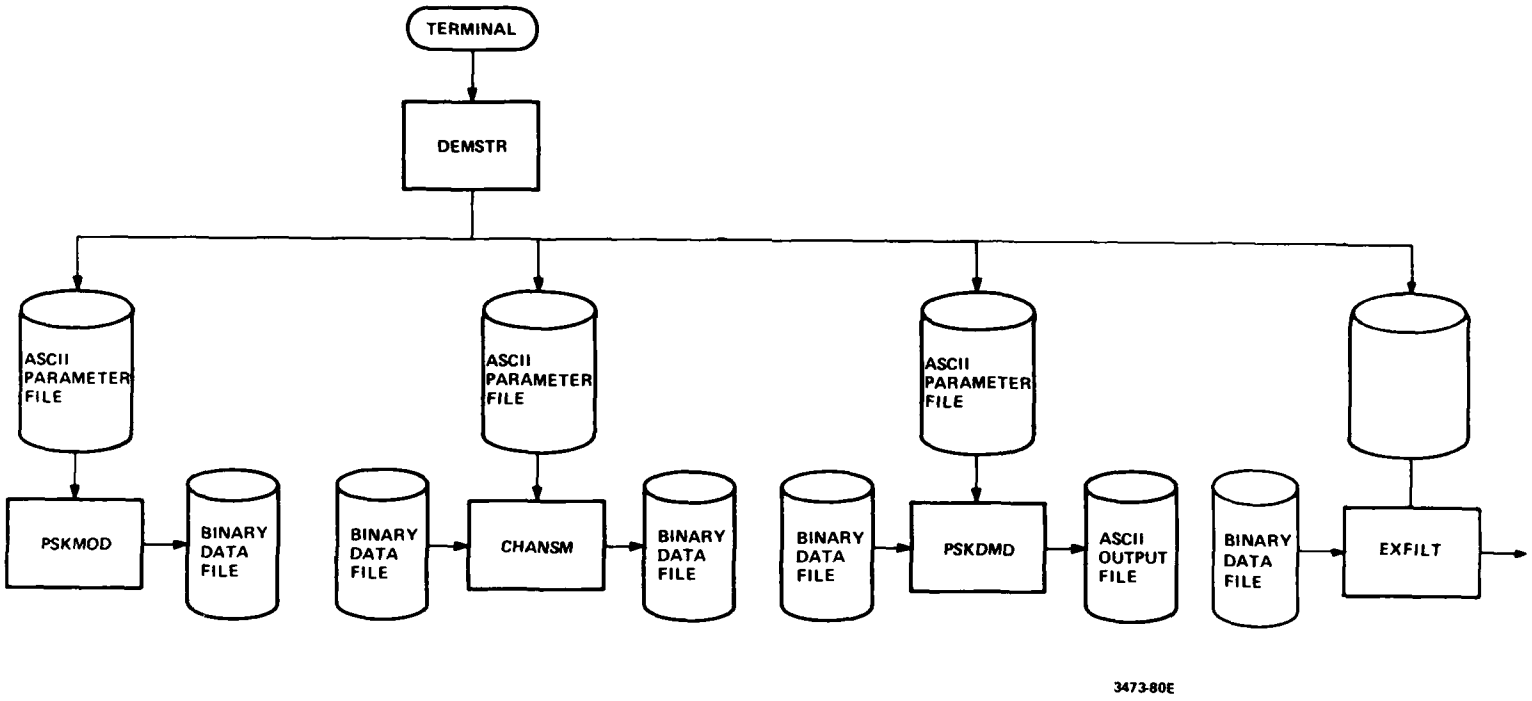

Figure 4-1. FORTRAN Simulation Software Organization

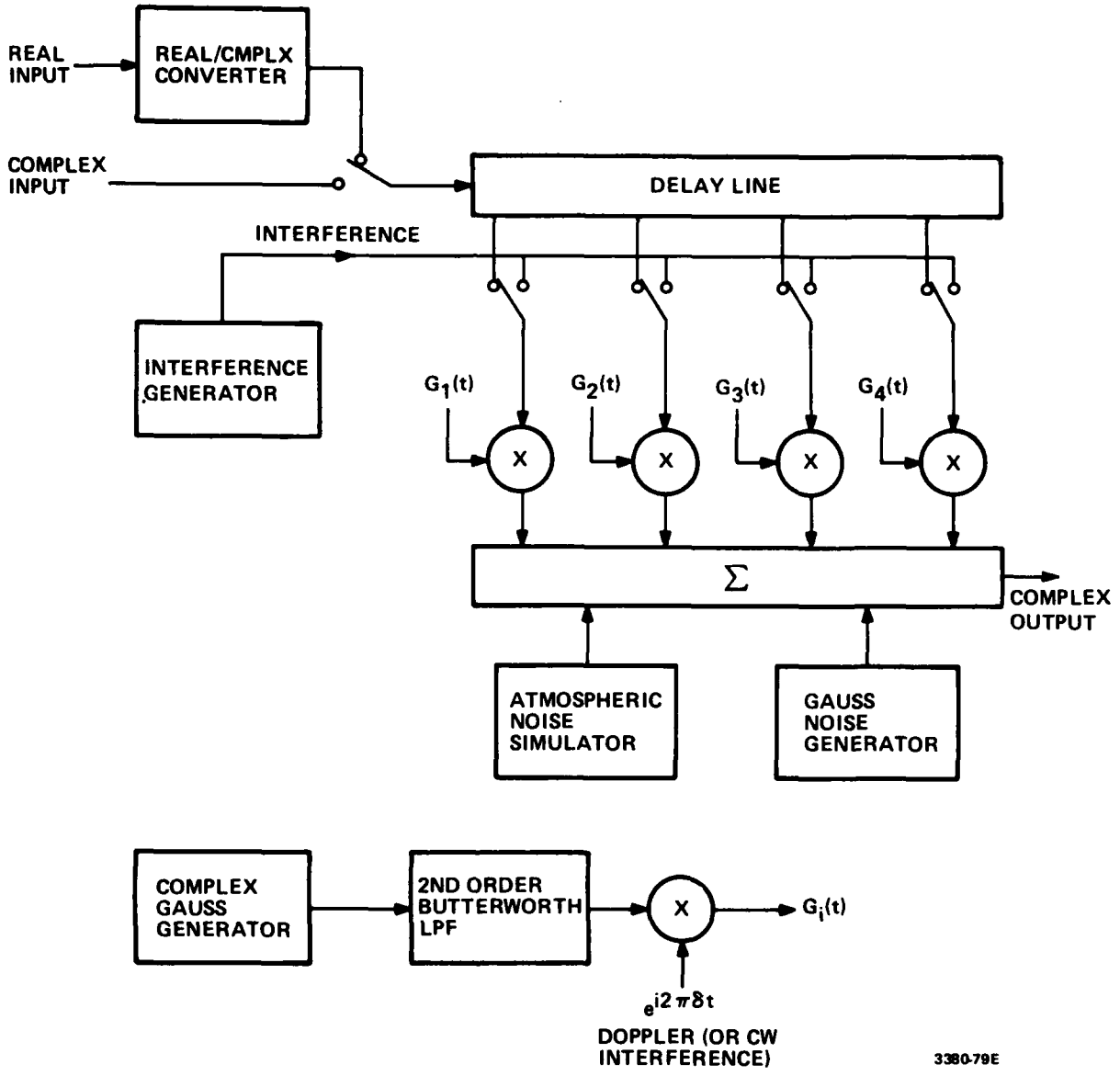

Figure 4-2. Block Diagram of HF Channel Simulation

PSKDMD simulates a demodulator implemented almost entirely in fixed precision arithmetic. The width of this precision is adjustable with its nominal value being 16 bits. PSKDMD produces statistics on input SNR, output SNR, error rates and time spent in the training mode. Carrier and clock synchronization algorithms are implemented as well as a decision feedback equalizer with Kalman updating. Also present is an initial acquisition algorithm as well as a mechanism to enter the training mode whenever the output SNR drops below a set threshold level. PSKDMD can accept as an input data file either the output of PSKMOD or CHANSM.

DEMSTR examines and updates the ASCII parameter files used by PSKMOD, CHANSM and PSKDMD. The use of parameter files greatly reduces the probability of operator error in inputting parameters.

4.2 Modem Performance

The FORTRAN simulation software described above was used as a testbed to investigate many aspects of the HFWBM design, including:

- Equalizer size requirements versus multipath distribution
- Fractional versus whole symbol spacing of the forward equalizer
- Quantization effects (especially as they relate to selection of the DFE adaptation algorithm)
- DFE/ART parameter optimization
- Error rate performance for fading and nonfading channels, different data rates, frequency offsets, timing jitter, etc.,
- Carrier tracking performance for frequency offsets and phase jitter

- Symbol synchronizer tracking performance.

The significant results from these simulations are highlighted in the paragraphs below.

4.2.1 Equalizer Size Requirements

It has been generally accepted that the feed-forward section of a DFE needs to span at least the total multipath spread, and that the feedback section should encompass one symbol period less than the time spanned by the feed-forward section. The terminology "total multipath spread" is meant to include the combined ISI effects of the HF propagation paths and bandlimiting filters in the radio equipment. Although in general these combined effects theoretically require an infinitely long equalizer, there is a point of diminishing returns as algorithm and quantization noise increase with equalizer size.

Simulations were conducted to determine the optimum equalizer size under a variety of combined filter, multipath and additive noise conditions. To simulate practical bandlimiting filters, a seventh order elliptic bandpass filter was placed between the modulator output and channel simulator input. Table 4-1 shows the filter design parameters that were chosen to approximate the audio bandpass characteristics of radio equipment conforming to MIL-STD-188C. Figure 4-3 indicates the ISI effects of this filter for 8-phase data before and after equalization. The discrete multipath characteristics that were investigated are listed in Table 4-2, and the optimum equalizer lengths that were found for both T-spaced and T/2-spaced DFEs are displayed in Table 4-3. Note that Channels 1, 2, 6 and 7 were fading at a 1 Hz rate, while Channels 3, 4 and 5 were nonfading.

TABLE 4-1. ELLIPTIC FILTER DESIGN PARAMETERS

Parameter	Value
Filter order	7
Passband ripple	.2 dB
Lower passband edge	250 Hz
Upper pass band edge	3100 Hz
Stopband attenuation	60 dB

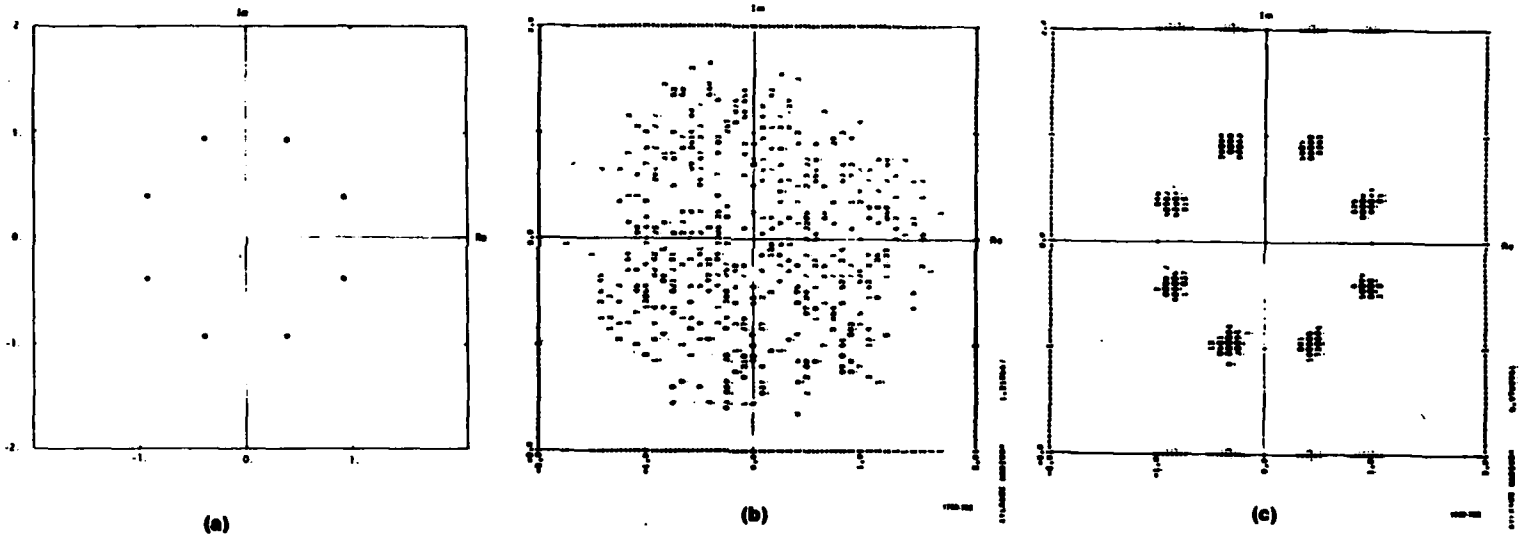

Figure 4-3. Phase Plots for 8-ϕ PSK Modem: (a) Transmitted Symbols, (b) Demodulated Symbols before Equalization, (c) After Equalization

TABLE 4-2. DISCRETE CHANNEL MULTIPATH CHARACTERISTICS

Channel No.	Description
1	Single path; 1 Hz. Rayleigh Fading
2	Two equal mean strength paths separated by .42 ms; 1 Hz Rayleigh fading
3	Two paths of amplitude 0 dB and -16 dB at relative delays of 0 and 1.25 ms, respectively; non-fading
4	Two equal amplitude paths at relative delays of 0 and 1.25 ms; non-fading
5	Two paths of amplitude -16 dB and 0 dB at relative delays of 0 and 1.25 ms, respectively; non-fading
6	Two paths of mean strength -16 dB and 0 dB at relative delays of 0 and 1.04 ms, respectively; 1 Hz Rayleigh fading
7	Three paths of mean strength -14 dB, 0 dB and -2 dB at relative delays of 0, .6 ms and 2.8 ms, respectively; 1 Hz Rayleigh fading

TABLE 4-3. OPTIMUM EQUALIZER SIZES FOR VARIOUS CHANNELS

	Optimum Equalizer	
Channel No.	T-Spaced	T/2-Spaced
1	(8,3)	(14,3)
2		(16,7)
6	(12,7)	(24,7)
7	(11,7)	(22,7)

The results obtained for the nonfading channels 3-5 are of interest because they provide some insight into equalizer size requirements for various steady-state conditions. These channels all have two discrete multipath components separated by three symbols, but they vary in amplitude distribution from minimum-phase (Channel 3) to linear phase (Channel 4) to nonminimum phase (Channel 5). In all cases the input SNR was 20.0 dB. The observed output SNRs (i.e., after equalization) for Channels 3, 4 and 5 and a (4,3) T-spaced DFE were 22.0 dB, 19.0 dB and 15.2 dB, respectively.* The steady-state equalizer tap weights for these three cases are shown in Figure 4-4. Note that the set of equalizer weights for the nonminimum phase channel (No. 5) do not decay appreciably over the span of the 7-tap DFE. Only by increasing the size of the equalizer was the performance of the nonminimum phase channel improved. Both 11-tap (8,3) and 15-tap (12,3) equalizers were able to bring the output SNR up to 21.5 dB. The steady-state tap weights for these equalizers with Channel No. 5 are also shown in Figure 4-4.

Since the HF channel will not always be minimum phase (as predictions in [2] indicate it frequently will not), the size of the equalizer should be expanded to include the expected multipath spread <u>plus</u> the impulse response of the radio filters. More precisely, a useful criterion would be to choose the minimum number of feed-forward taps m that satisfies

$$\sum_k |f_k|^2 |h(mT - \tau_k)|^2 \leq 3 \times 10^{-3}$$

for a T-spaced equalizer, or

$$\sum_k |f_k|^2 |h(mT/2 - \tau_k)|^2 \leq 3 \times 10^{-3}$$

*For simplicity, we use the notation (n,m) to indicate a DFE with an n forward taps an m feedback taps.

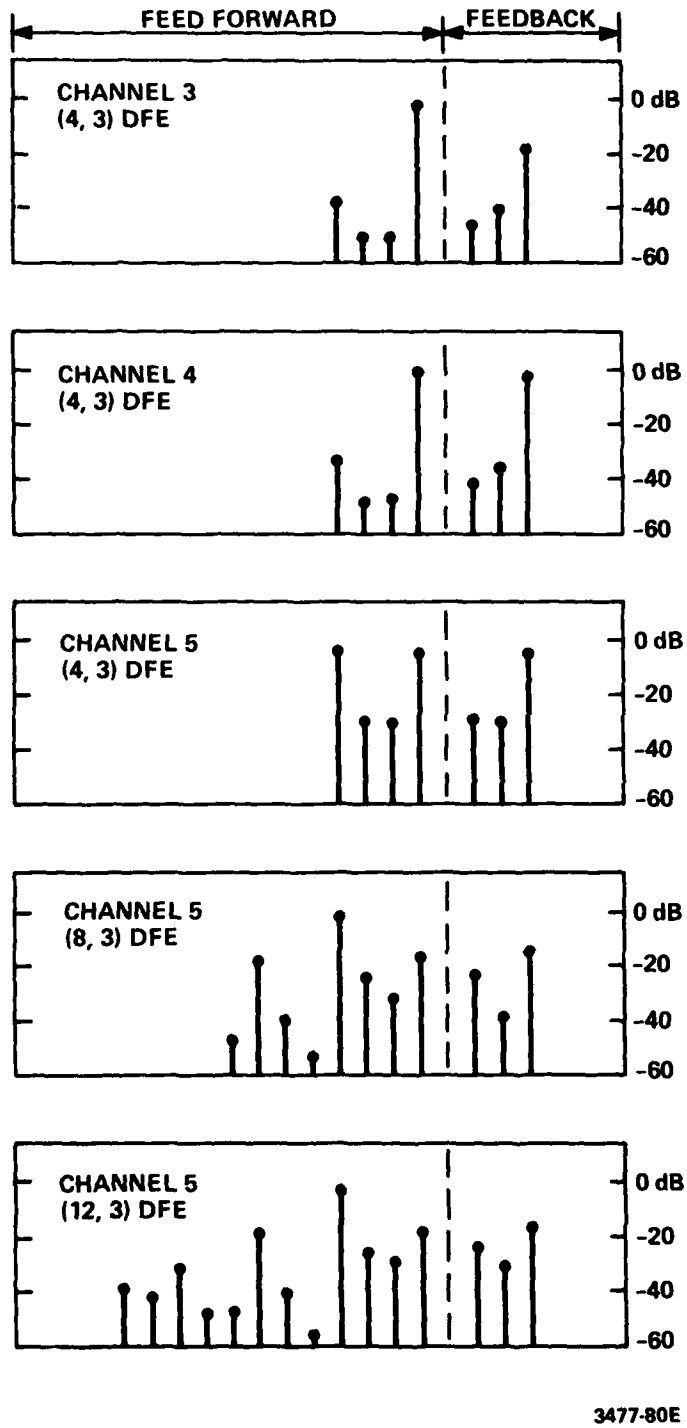

Figure 4-4. Steady State Equalizer Tap Distributions

for a T/2-spaced equalizer. In the above expressions, f_k^2 represents the strength of the k-th multipath component arriving at delay $_k$, the delay $_k$ is measured relative to the earliest arriving component that is within -25 dB of the strongest component, and $h(t)^2$ represents the squared envelope of the low pass equivalent filter impulse response. The -25 dB threshold (also commensurate with the right hand of the above inequalities) represents a level at which ISI can be effectively ignored without affecting modem performance (e.g., for up to 16-phase keying at 10^{-3} error rate). The upper limit in the summation over k needs to include only those terms where f_k^2 is within -25 dB of the strongest component.

4.2.2 T versus T/2 Equalizer Spacing

A T-spaced DFE is known to be somewhat less sensitive to synchronization errors than is a linear equalizer. Also, a T/2-spaced linear equalizer is known to be less sensitive to timing errors and to offer better performance than a T-spaced linear equalizer. Our simulations have shown that a DFE operated with a T/2-spaced feed-forward section provides the best error rate performance and is almost completely insensitive to symbol timing phase. Figures 4-5 and 4-6 show some of the results.

The data in Figure 4-5 were obtained for the nonfading channel disturbed only by the seventh-order elliptic filter. The output SNR for the T/2-spaced DFE varies by less than 1 dB as the timing phase is moved over a complete symbol period. The corresponding variation for a T-spaced DFE is 4 dB. The data in Figure 4-6 were obtained for the combined elliptic filter and a two-path fading channel having a multipath distribution as described in Table 4-2 for channel No. 6. The error rate versus SNR for this 4-phase data (4800 b/s) displays a flattening out at high SNR for the case of a (12,7) T-spaced

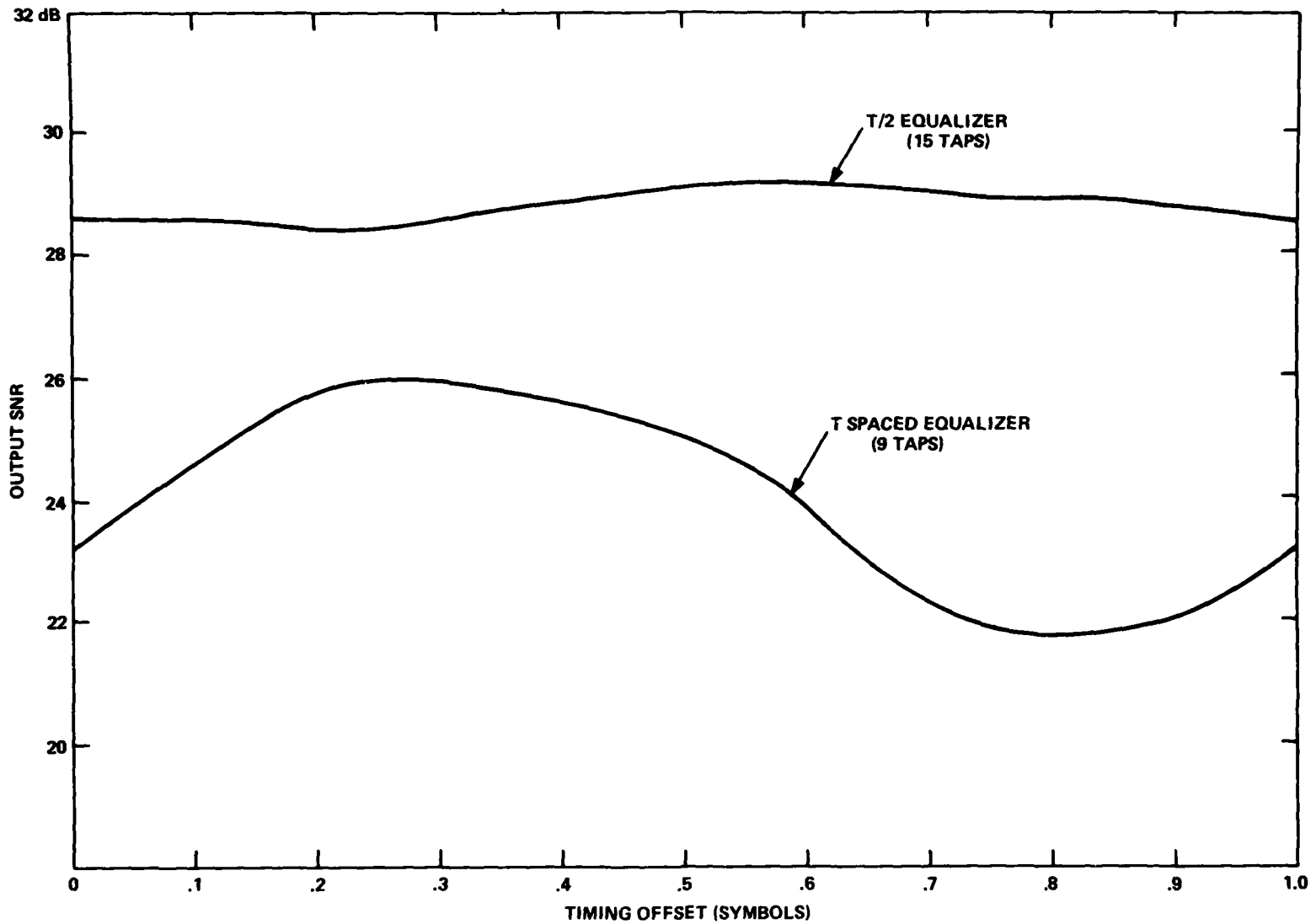

Figure 4-5. Output SNR versus Timing Offset for T and T/2-Spaced Decision Feedback Equalizers

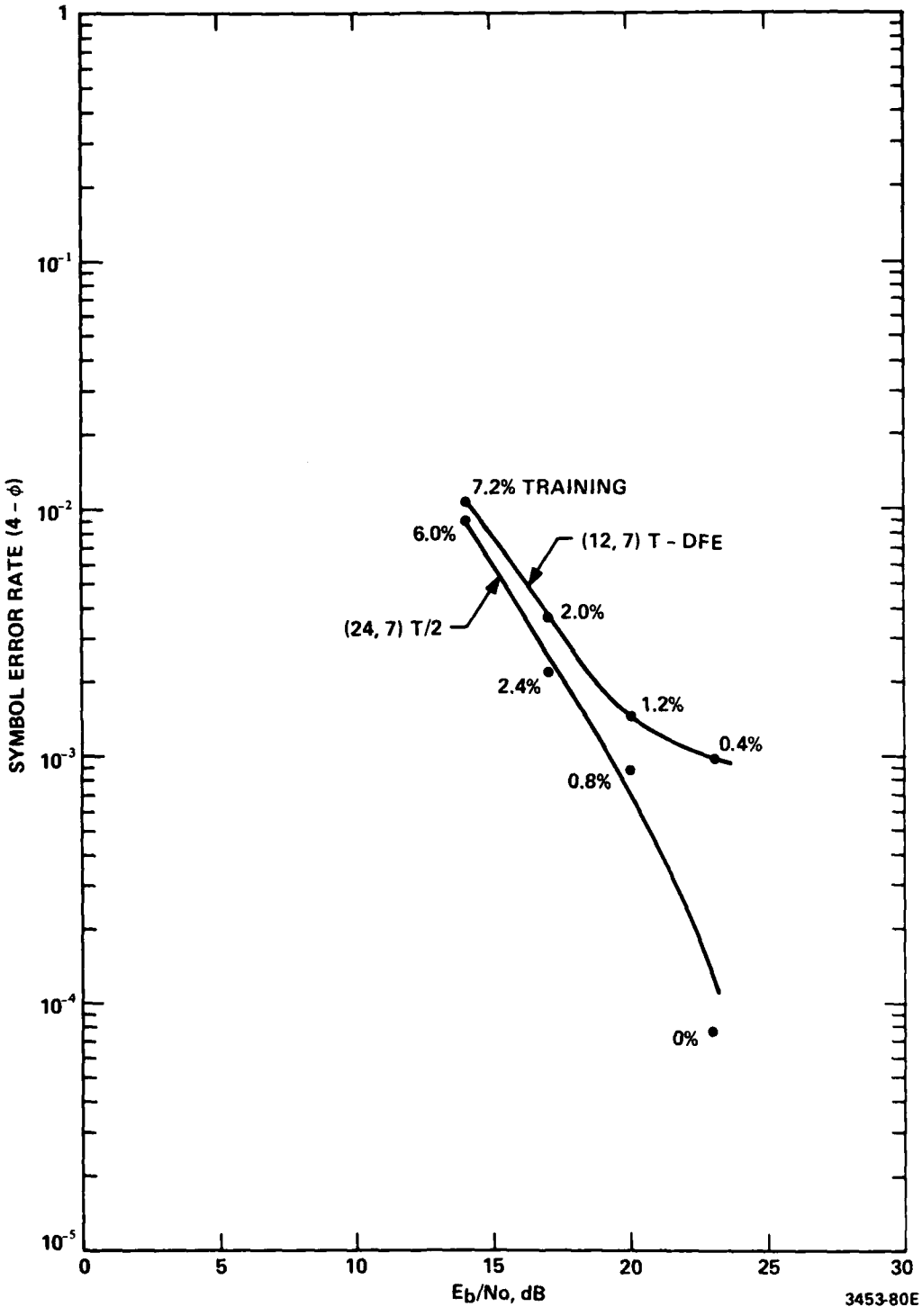

Figure 4-6. Comparison of Simulation Results of T- and T/2-Spaced DFEs with 4800 b/s Data on Two Path Fading Channel

equalizer. The percentages shown adjacent to each data point in Figure 4-6 indicate the amount of training requested by the ART system. It is observed that, along with better error rate performance, the T/2-spaced equalizer generally requires less training.

The simulation results clearly indicate that a T/2-spaced DFE is preferred over a T-spaced feed-forward section that will span up to 5 ms total multipath spread. When a longer equalizer is required, the HFWBM can be switched to a T-spaced DFE mode wherein a total spread capability of up to 7.5 ms. is available. In either case, the number of feed-forward and feed-back taps are operator selectable.

4.2.3 Quantization Effects

An early analysis indicated that the limiting output SNR due to quantization effects alone would be about 32 dB if the HFWBM were implemented in a 16-bit fixed point processor. The principal issues that remained to be explored via simulations were the algorithm self-noise associated with the equalizer adaptation process and the extent to which computer round-off errors impact the stability of adaptation algorithm. These issues were separated by first testing candidate algorithms in a floating point simulation and then testing in fixed point simulations with decreasing computer word sizes.

The results of floating point simulations indicated the error rate performance curve for the conventional Kalman algorithm lies within about 1.5 dB of the theoretical tap weight curve when both are evaluated for a two-path Rayleigh fading channel. Floating point simulations also showed that the "fast Kalman" algorithm was unstable for time-varying channels. Thus, the floating point performance of the conventional Kalman algorithm became the

baseline for assessing the performance of adaptation algorithms in fixed point simulations.

The fixed point simulations demonstrated a need to operate the conventional Kalman algorithm with at least 20-bit precision arithmetic in order to achieve good error rate performance for the two-path fading channel. These results prompted a two-pronged effort to define a solution for the HFWBM. First, an architecture study was initiated for a 24-bit processor capable of performing the conventional Kalman algorithm. Second, a square-root formulation of the Kalman algorithm was implemented in the fixed-point simulation.

The fixed-point square-root Kalman algorithm simulations were successful. It was found that implementation of this algorithm in 16-bit arithmetic gave similar performance to the 24-bit implementation of the conventional Kalman algorithm. It was also found that the accumulation of round-off errors in both algorithms could be minimized by periodically resetting the error covariance matrix to a diagonal form. However, the square-root algorithm was found to be the only acceptable 16-bit solution for long equalizers (i.e., up to 35 taps). A performance comparison between the final fixed-point and equivalent floating point square-root algorithms is indicated in Figure 4-7. The combination of all quantization effects are observed to cause about a 2 dB degradation in the error rate performance.

It should be noted that considerable effort was devoted to developing an optimum scaling strategy which simultaneously minimizes quantization noise and prevents fixed point overflows. The scaling strategy finally selected played a key role in achieving successful operation of the HFWBM in 16-bit fixed-point arithmetic. The details of this strategy are documented in the Program Maintenance Manual for the FORTRAN simulation software [21].

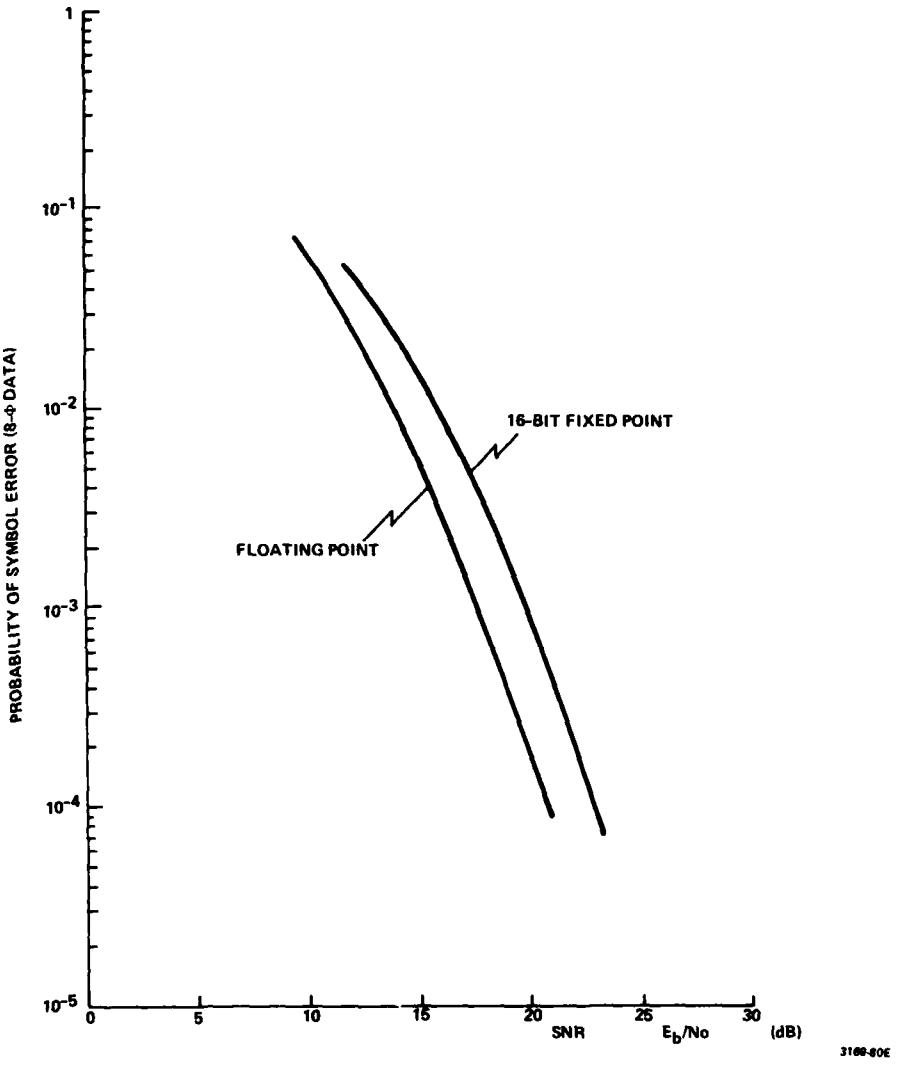

Figure 4-7. Comparison of 16-Bit and Floating Point Performance of Square-Root Kalman Algorithm for Two-Path Fading Channel, DFE (4,1)

4.2.4 Parameter Optimization

In addition to the scaling strategy, a number of control parameters affecting the overall performance of the HFWBM were optimized in the course of exercising the fixed-point simulation software. Table 4-4 lists some of the more important parameters and their optimized values.

Low reset rates (large values of NRSET) can lead to numerical instabilities (fixed point overflows), particularly for large size equalizers. High reset rates (small values of NRSET) lead to degraded error rate performance. The optimum of one reset every 100 symbols was obtained for a (16,7) T/2 DFE operating with fading channel No. 2.

The AGC time constant is given approximately by T/(1-AGCCN). If the AGC is too slow (values of AGCCN near unity), the equalizer will try to compensate for signal fades. This can lead to numerical difficulaties in the fixed-point implementation. Conversely, if the AGC is too fast (small values of AGCCN), ISI will be introduced as the AGC tries to follow envelope variations due to the random data pattern. The value of AGCCN = 0.98 was obtained from experience with fading channel No. 2.

DINIT and QINIT are two parameters that control the stability and convergence rate of the adaptive equalizer. The performance of the final square-root Kalman algorithm is relatively insensitive to the choice of DINIT. Larger values of QINIT generally provide faster convergence; however, fixed-point overflows occur if QINIT is made too large. Also, the optimum value of QINIT depends somewhat on NRSET and the size of the equalizer. The value QINIT = 0.03 appears to be a good compromise for NRSET = 100 and the contemplated range of equalizer sizes. A potential refinement exists for short

TABLE 4-4. OPTIMIZED VALUES FOR CRITICAL PARAMET

Parameter Name*	Optimized Value
NRSET	100
AGCCN	.98
DINIT	1.0
QINIT	.03
EQLCN	.98
THRDB	7-10

*As used in [21]

equalizers where QINIT can be made somewhat larger wihout getting into any fixed point overflows.

The time constant for the output SNR monitor is given approximately by T/(1 - EQLCN). If this monitor is too sluggish (values of EQLCN near unity), error rate performance will be degraded by delays in ART/ARQ responses to signal fades. If the monitor is too fast (small values of EQLCN), throughput efficiency will drop due to excessive requests for training.

The SNR threshold for automatically requesting training (ART) is determined by the parameter THRDB. The higher this threshold is set, the more frequent will be ART. This tends to lower error rates at the expense of throughput efficiency. Conversely, lower values of THRDB afford higher throughput at the expense of higher error rates. A compromise must be reached between efficiency and error rate objectives. Figure 4-8 shows the results of simulations which demonstrated that 6 dB and 10 dB were reasonable choices for THRDB for 4800 b/s and 7200 b/s, respectively. The dependence of optimum THRDB on data rate could be lessened by using a monitor which measures SNR per bit rather than the symbol SNR. The effect of using a fixed percent training rather than ART is shown in Figure 4-9. Such a scheme is clearly inferior because training is sometimes requested when it is not needed (lowers efficiency) and is sometimes not requested when it is needed (increases error rate). No attempt was made to optimize the fixed percentage training. The single choice of 2.8 percent was made in an effort to achieve a middle ground in the range of training rates observed in the ART simulations. All data in Figures 4-8 and 4-9 used fading channel No. 6.

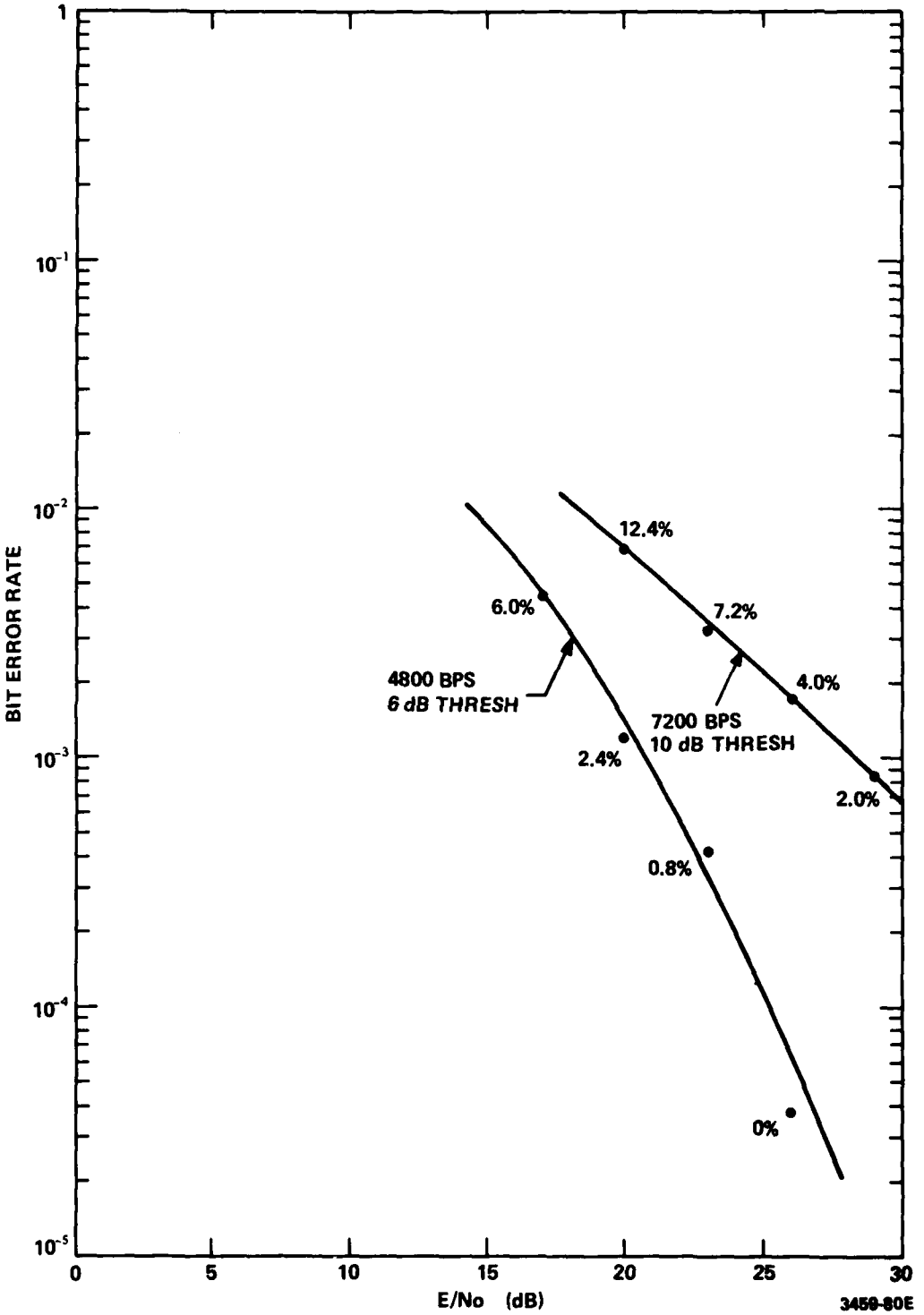

Figure 4-8. Simulation Results for T/2 (24,7) Equalizer on Two-Path (.025, 1.0) Fading Channel

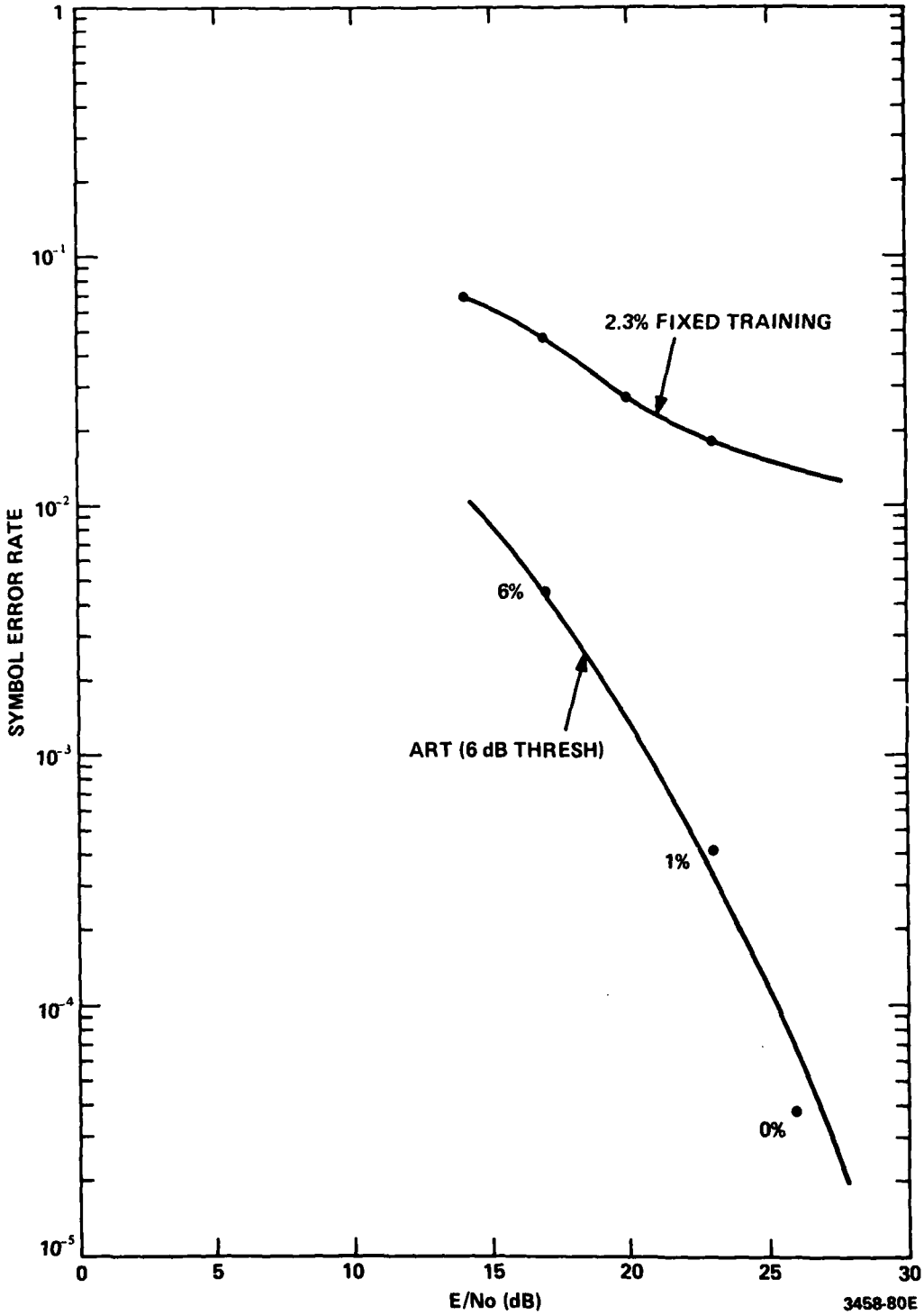

Figure 4-9. Simulation Results for T/2 (24,7) Equalizer on Two-Path (.025, 1.0) Fading Channel. 4800 b/s with ART (6 dB Thresh) and Fixed 2.8 Percent Training

4.2.5 Error Rate Data

This section highlights some of the overall error rate performance data obtained for the 16-bit simulation of the HFWBM employing the selected square-root Kalman DFE adaptation algorithm. More detailed data on variants to or specific parts of the recommended design can be found elsewhere in this report.

First, the error rate performance for four different data rates on a nonfading channel is shown in Figure 4-10. The nonfading channel includes a seventh-order elliptic bandpass filter, and the equalizer in all cases is a (14,3) T/2-spaced DFE. The measured performance for all data rates was within 1.5 dB of the theoretical performance for an ideal matched filter.

Next, the error rate performance for 8-phase (7200 b/s) data on various 1 Hz fading channels was obtained. Simulation results for fading channels 2 and 6 are presented in Figure 4-11. Additional error rate performance data were obtained for 4-phase (4800 b/s) data on fading channels. Simulation results for fading channels 6 and 7 are displayed in Figure 4-12.

4.2.6 Carrier Tracking Performance

Floating point simulation results which demonstrate the performance of the carrier tracking algorithm are presented in [5]. It was found that the error rate performance with the carrier tracking algorithm ON suffers only about 0.3 dB degradation relative to the ideal performance for a 10 Hz frequency offset and fading channel No. 2. Acquisition of up to 100 Hz frequency offset was also demonstrated. The algorithm was shown to be capable of following moderate amounts of phase jitter for short equalizers. Although strong phase jitter is not expected to be a problem in the HFWBM application,

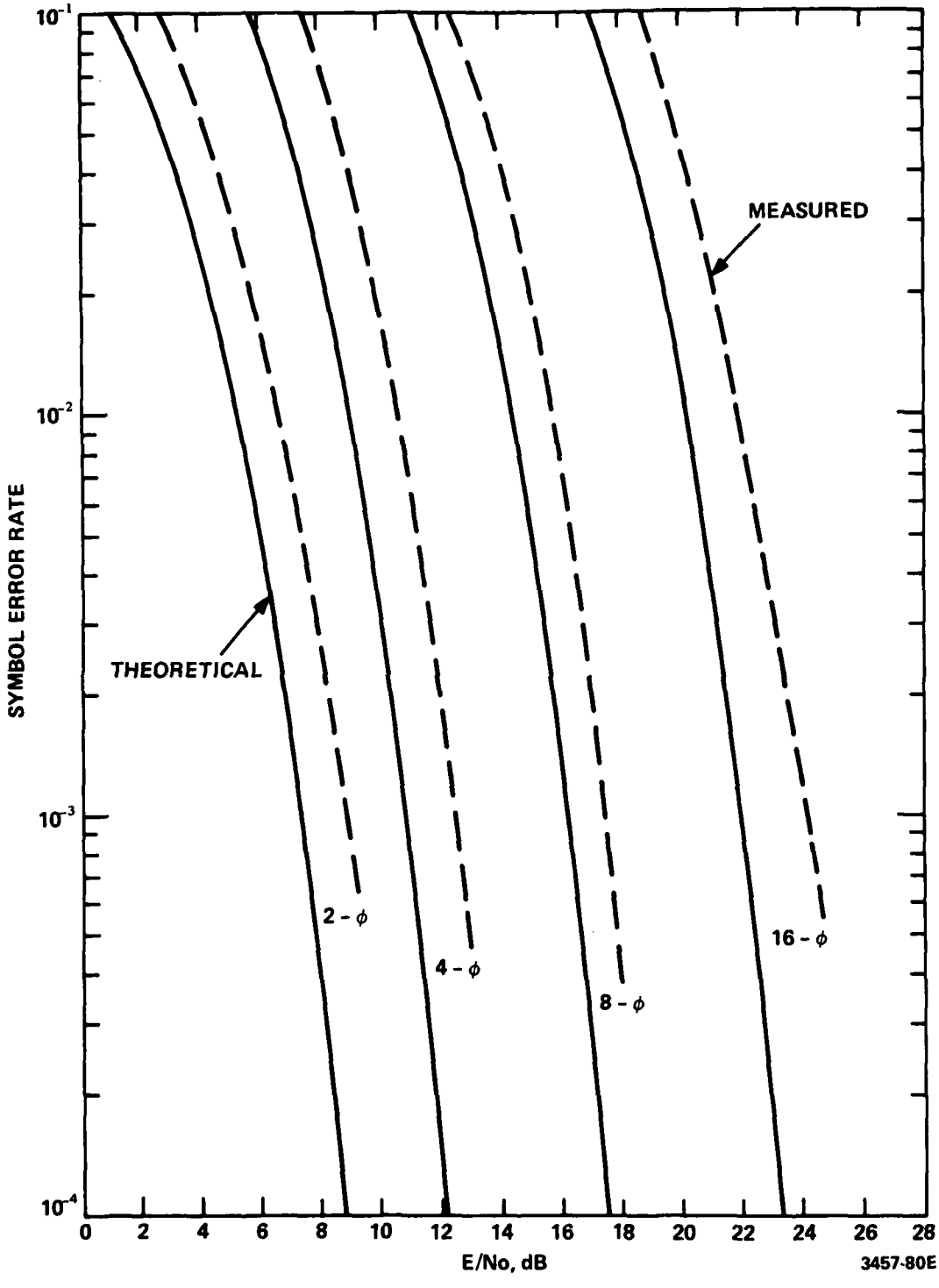

Figure 4-10. Square-Root Kalman Algorithm Nonfading Test Results

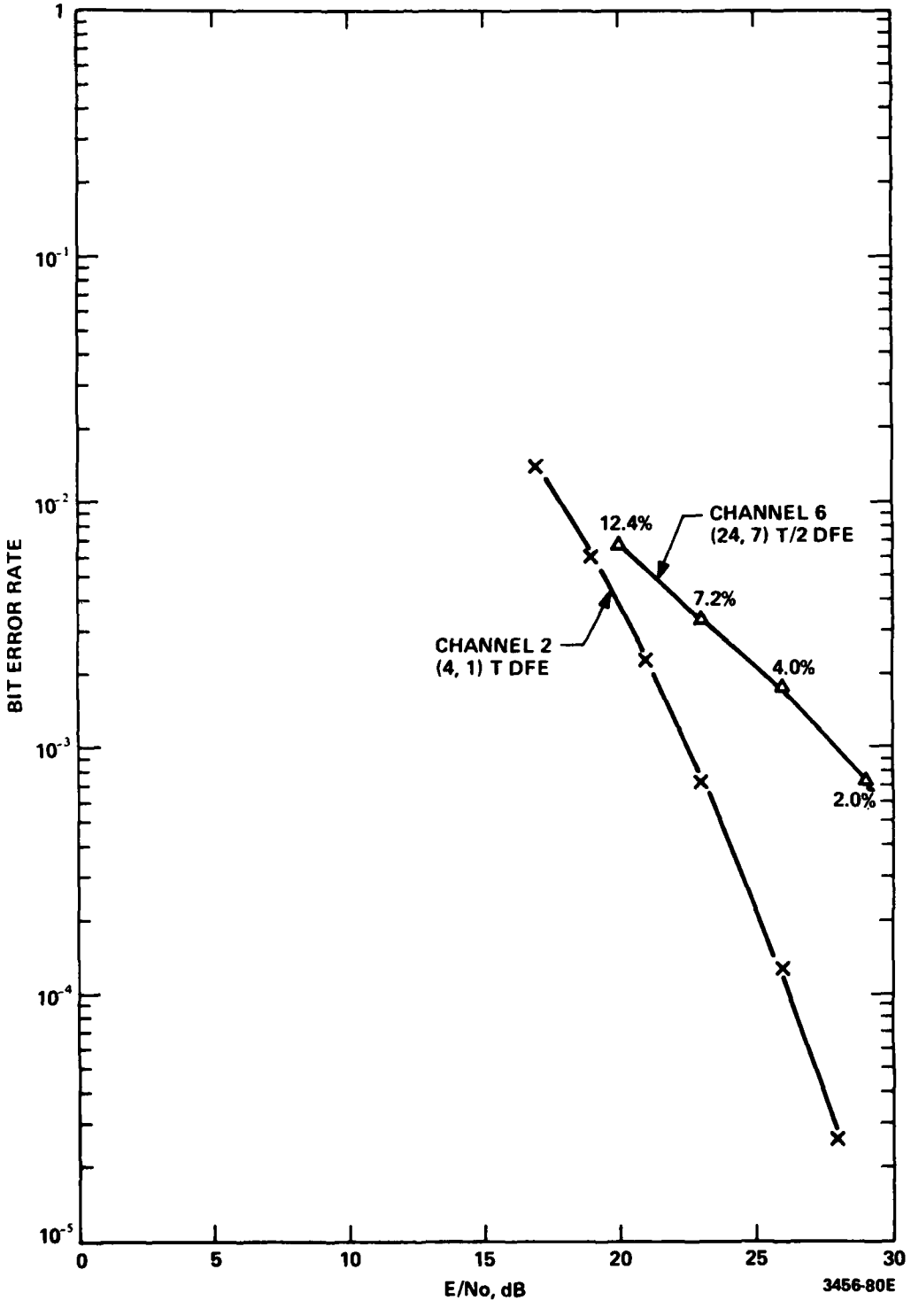

Figure 4-11. Bit Error Rate versus Signal-to-Noise Ratio for 7200 b/s and Fading Channels 2 and 6

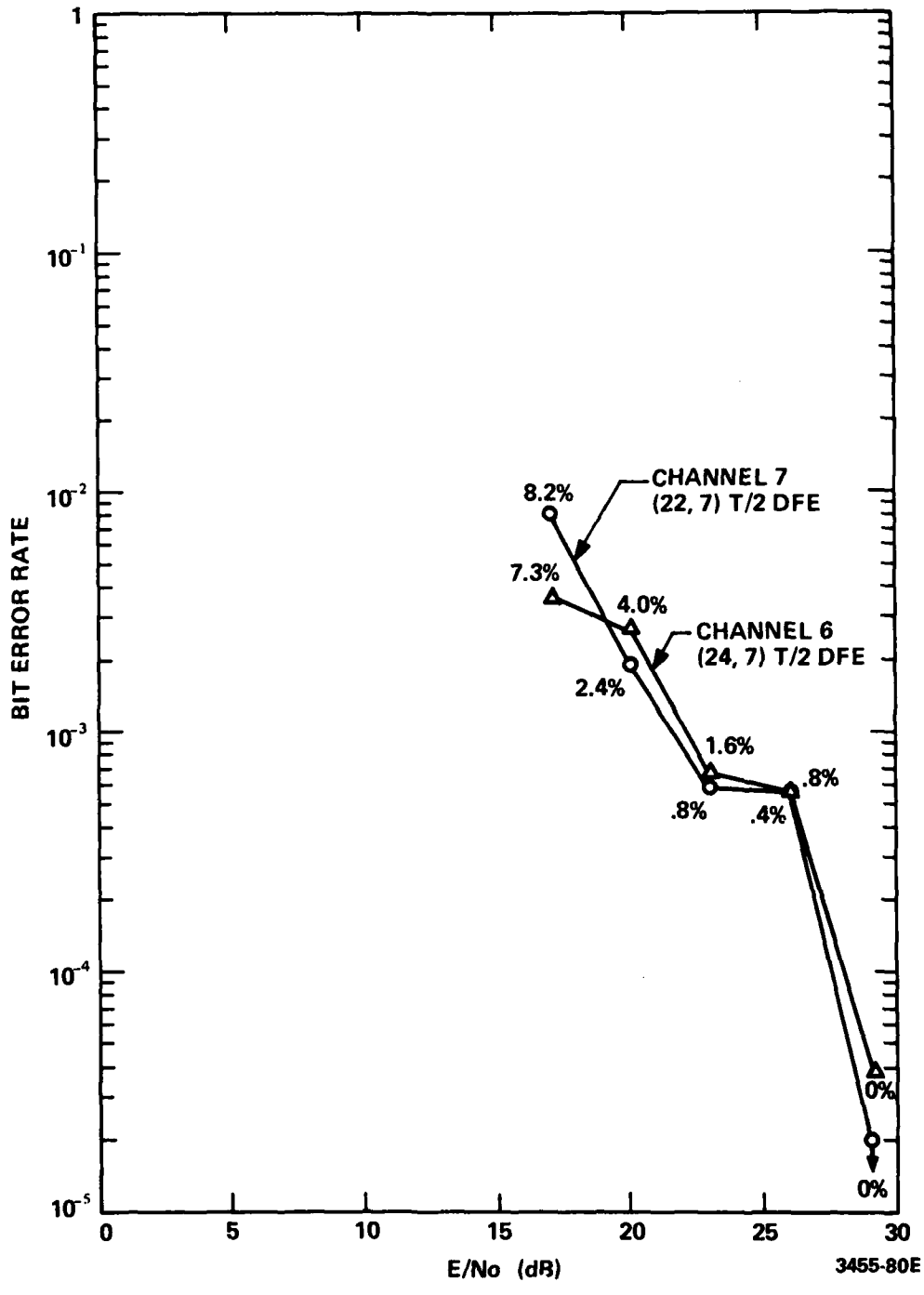

Figure 4-12. Bit Error Rate versus Signal-to-Noise Ratio for 4800 b/s and Fading Channels 6 and 7

the algorithm could be easily modified to handle this case by adding a phase correction loop to the output of the equalizer.

4.2.7 Symbol Synchronizer Performance

Simulation results which demonstrate the performance of the symbol syncrhonizer algorithm on a nonfading channel with ISI and carrier offset are given in [6]. It was found that the error rate performance with the syncrhonizer ON suffers a degredation of only about 0.2 dB relative to the performance with perfect fixed synchronization. Carrier offsets up to 240 Hz were shown to have negligible effect on synchronizer performance. To fully stress the algorithm under fading channel conditions, a special multipath fading channel was used. This special channel began with a period of a single component which slowly faded toward zero amplitude as a second component at 2-1/2 symbols delay simultaneously increased from zero to unity amplitude. The simulation results for this channel demonstrated the ability of the synchronizer to maintain proper sync without any cycle skipping.

5.0 REAL-TIME HARDWARE DESIGN

5.1 Overview

To implement the HF Wideband Modem in hardware, a functional split has been made in the algorithm between those sections to be executed in the GTE Sylvania Systems Group Mark IV Signal Processor, and those to be executed in the Kalman Signal Processor (KSP). This split is commensurate with the capabilities and performance of each unit. The Mark IV processor is a self-contained audio signal encoder/synthesizer with A/D, D/A, RS-232C, and 188C interfaces. It has been used in a variety of applications, including Linear Predictive and Adaptive Predictive Coding Digitizers, data encryptors, HY-2 compatible Vocoders, and a number of HF modems. Its internal processing element, memory, and data conversion resouces make it ideal to perform all the functions of the HF Wideband Modem, except for the Kalman update algorithm which requires very high speed manipulation of data arrays, rapid complex number multiplication, and reciprocal generation. The KSP which implements those latter operations represents a particular embodiment of a High Speed Signal Processor (HSSP) developed by GTE Sylvania Systems Group under independent development.

A decision feedback equalizer, implemented with 35 taps and employing a square-root Kalman algorithm for updating tap weights, requires the following operations per symbol:

a. 2206 Complex multiplies

b. 1961 Complex adds

c. 36 Real reciprocals.

An array processor that could handle these operations serially at 2400 baud would require an instruction execution rate of over 10 MHz. Alternatively, the instruction execution rate could be as low as 5.3 MHz if all three types of operations would occur simultaneously.

A survey of the array processor industry, summarized in Table 5-1, indicated the Westinghouse PSP-X^{+} as the only processor with adequate computational speed to operate as a KSP other than the GTE HSSP. The Westinghouse machine was not selected because of its physical size (2 racks) and cost ($283K+). Instead, a GTE designed array processor designated the HSSP was chosen because it possesses the necessary speed in a more compact and lower cost implementation.

Figure 5-1 shows the high-level equipment configuration comprising the HF Wideband modem. The Mark IV processor performs A/D and D/A conversions, modulation, sync acquisition, carrier tracking, and the symbol decision, decoding, and ARQ functions. It also serves as the host processor to the KSP, which executes the square root Kalman update algorithm. The Mark IV also provides an RS-232C interface to the Data Terminal Equipment (DTE).

The KSP, with its multiple bus structure and powerful computational abilities, executes the Kalman algorithm under Direct Memory Access (DMA) control from the Mark IV. The Kalman algorithm requires manipulation of arrays of 32-bit complex numbers, with such operations as vector-matrix multiplication and reciprocal generation. In real-time, this processor operates in parallel with the Mark IV host processor. Figure 5-2 shows a block diagram of the Sylvania Systems Group Mark IV processor. A detailed diagram and description of the KSP appears in the following section of this report.

TABLE 5-1. ARRAY PROCESSOR SURVEY

Manufacturer	Model	Word Size and Format	Execution Time (ns)					Programming Method	Data Memory Size	Single Instruction Capability	Interface	Price	Delivery
			Real Add	Real Multiply	Cmplx Add	Cmplx Multiply	Instr Cycle						
Stein Associates	AR-10/10 (1-DDS)	16 Bit Fixed Point	142.9	285.8	285.8	1143.2	142.9	RAM Downloaded from Host	DDS: 8Kx16 Real PAS: 4Kx16 Cmplx	DDS: 1 Add or 1/2 Mult PAS w/1AE: 2 Mult, 4 Add 2 Mem Acc PAS w/2AE: 4 Mult, 8 Add 4 Mem Acc	PDP-11 NOVA	$ 38,000	60 DA
	AR-10/11 (1-DDS 1-PAS w/1AE)		71.5	142.9	142.9	571.6	DDS: 142.9 PAS: 285.8					$ 75,000	120 DA
	AR-10/12 (1-DDS 1-PAS w/2AE)		35.8	71.5	71.5	285.8						$ 95,000	120 DA
	AR-10/22 (1-DDS 2-PAS w/2AE)		35.8	71.5	71.5	285.8						$125,000	120 DA
Signal Processing Systems	SPS-81	16 Bit Fixed Point	83.33	125	250	500	500	RAM Downloaded from Host		1 Cmplx Mult and 2 Cmplx Add	PDP-11 LSI-11	$ 50,000	60-90 DA
Computer Design and Applications	MSP-3	24 Bit Block Float Point	216.7	650			2600	PROM	4K x 24	4 Mult, 12 Add	PDP-11	$ 14,200	30-60 DA
Analogic	AP-400	24 Bit Block Float Point	160	480			1920	RAM Downloaded from Host	4K x 24	4 Mult, 12 Add	PDP-11 NOVA	$ 12,500	60 DA
CSPI	MAP-100	32 Bit Floating Point	1600	1600			1600	RAM		1 Mult then 1 Add		N/A	N/A
	MAP-200		210	420			420		One 256 x 16	1 Mult and 2 Add		$ 22,350	60 DA
	MAP-300		105	210			420		Two 256 x 16	2 Mult and 4 Add		$ 26,950	60 DA
Westinghouse	PSP-X+	16 Bit Fixed Point	100	100	100	100	100	RAM	Six 1K x 32	Pipeline (N+3) 100 ns Cmplx or Real		$285,000+	210 DA
CNR		16 Bit Fixed Point	110	220	110	220		PROM	8k x 16 Cmplx		PDP-11 LSI-11	N/A	N/A
GTE Sylvania Systems Group	HSSP	16 Bit Fixed Point	140	140	140	140	140	PROM	Three 1K x 32	Simultaneous Multiply ALU Reciprocal	MARK IV	N/A	N/A

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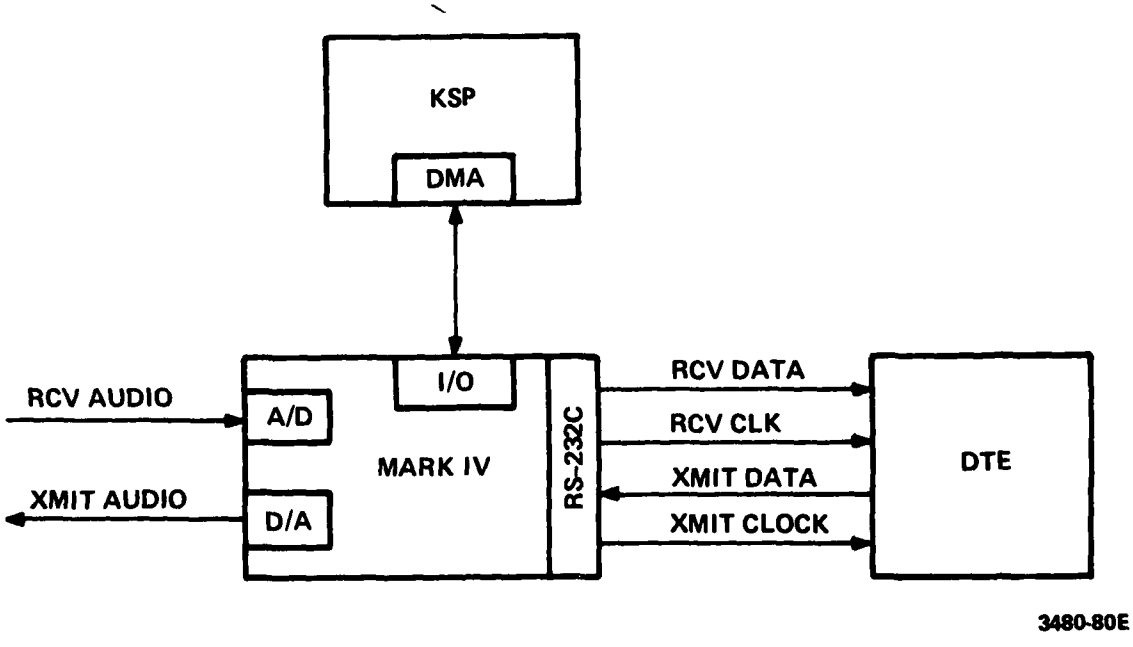


Figure 5-1. HF Wideband Modem Full Duplex Configuration

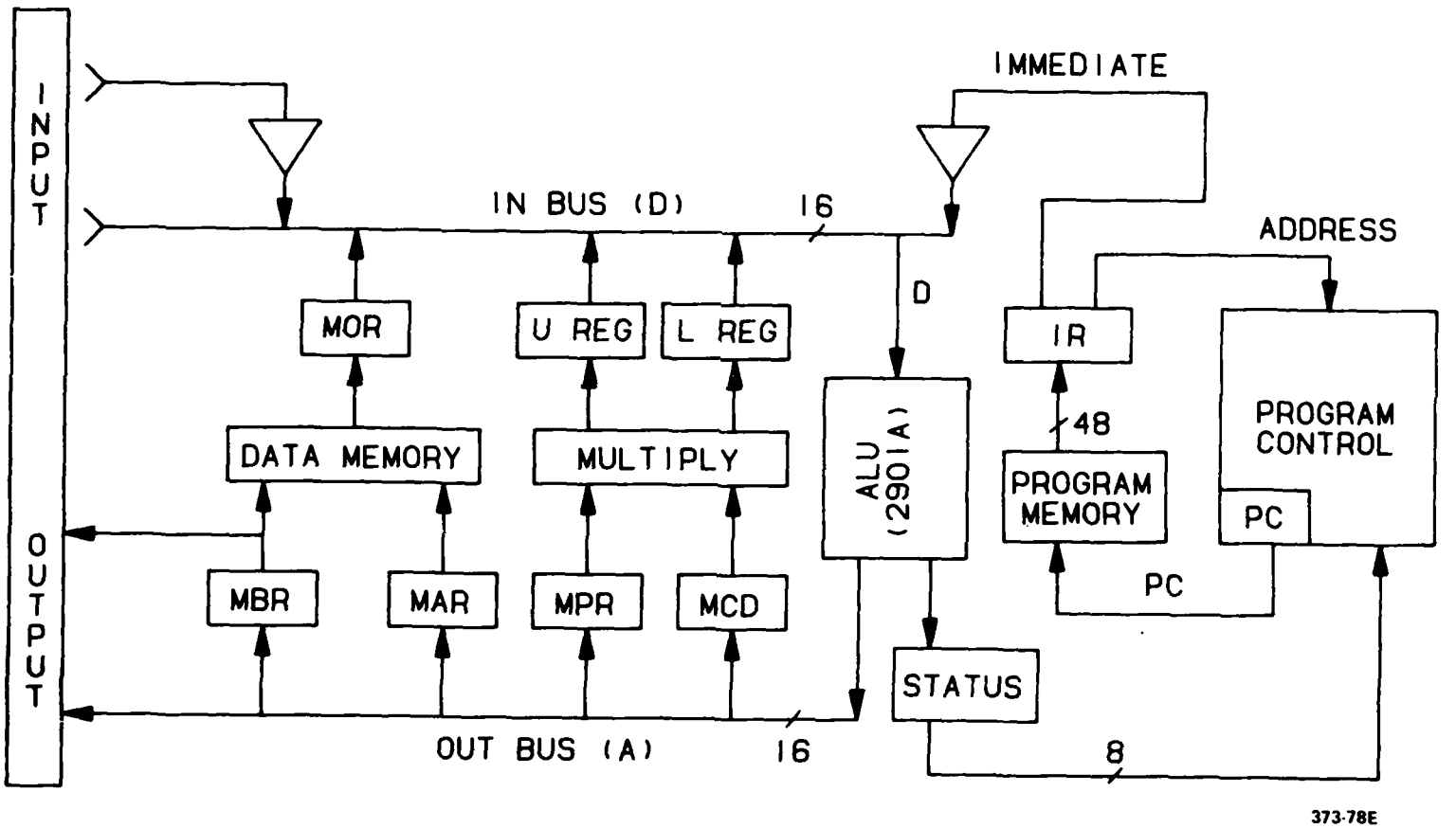


Figure 5-2. Mark IV Block Diagram

5.2 KSP Design

5.2.1 KSP Architecture

Figure 5-3 depicts the architecutre of GTE Sylvania Systems Group High Speed Signal Processor (HSSP) being used in the HF Wideband Modem as the Kalman Signal Processor (KSP). The machine is characterized by a multi-bus parallel architecture operated in a fully synchronous mode, three separate data memories allowing highly efficient data flow, a complex multiplier, ALU, and a real reciprocal generator. All three data memories each have their own address processor. Data Memory 1 is provided with a DMA interface to the Mark IV host processor. Additional features of the processor include:

- 32-bit complex operands
- Synchronous operation, all elements operate and perform a function within one machine cycle (140 ns)
- A complex multiplier accepts two complex operands and produces a scaled complex product each machine cycle
- A complex ALU performs one complex add, subtract, or logical operation per machine cycle
- Each data memory is capable of one read or write every machine cycle.

The 3-bus architecture is ideal for execution of the square-root Kalman algorithm with its requirement for data array operations and many intermediate calculations. The X and Y buses can be driven by all three data memories so that operations between Memory 2 and Memory 3 can be implemented directly.

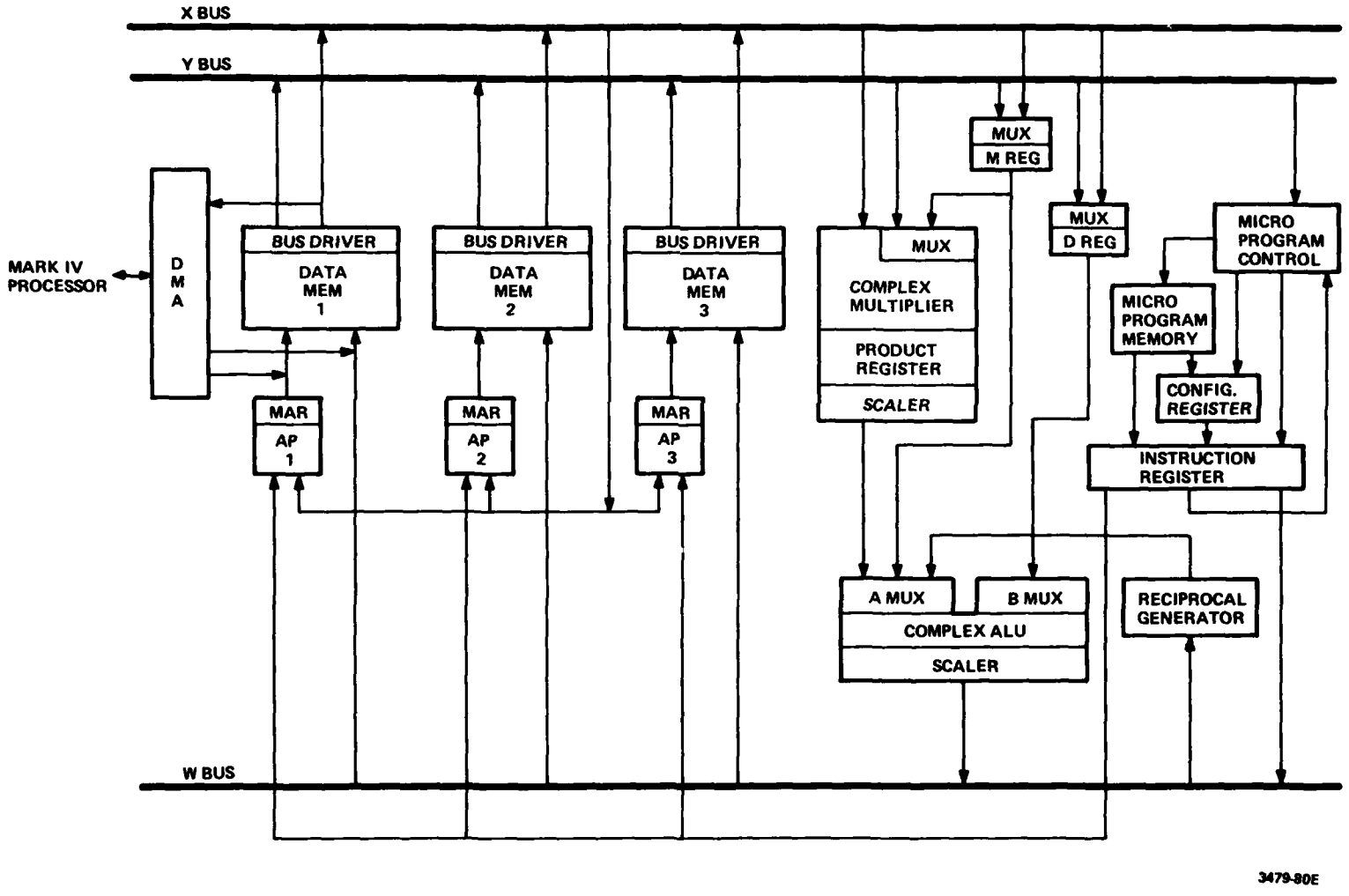


Figure 5-3. High Speed Signal Processor

The M register can be loaded from both the X and Y buses and, therefore, from any memory. The W bus serves as the destination for arithmetic outputs and the source for data memory inputs.

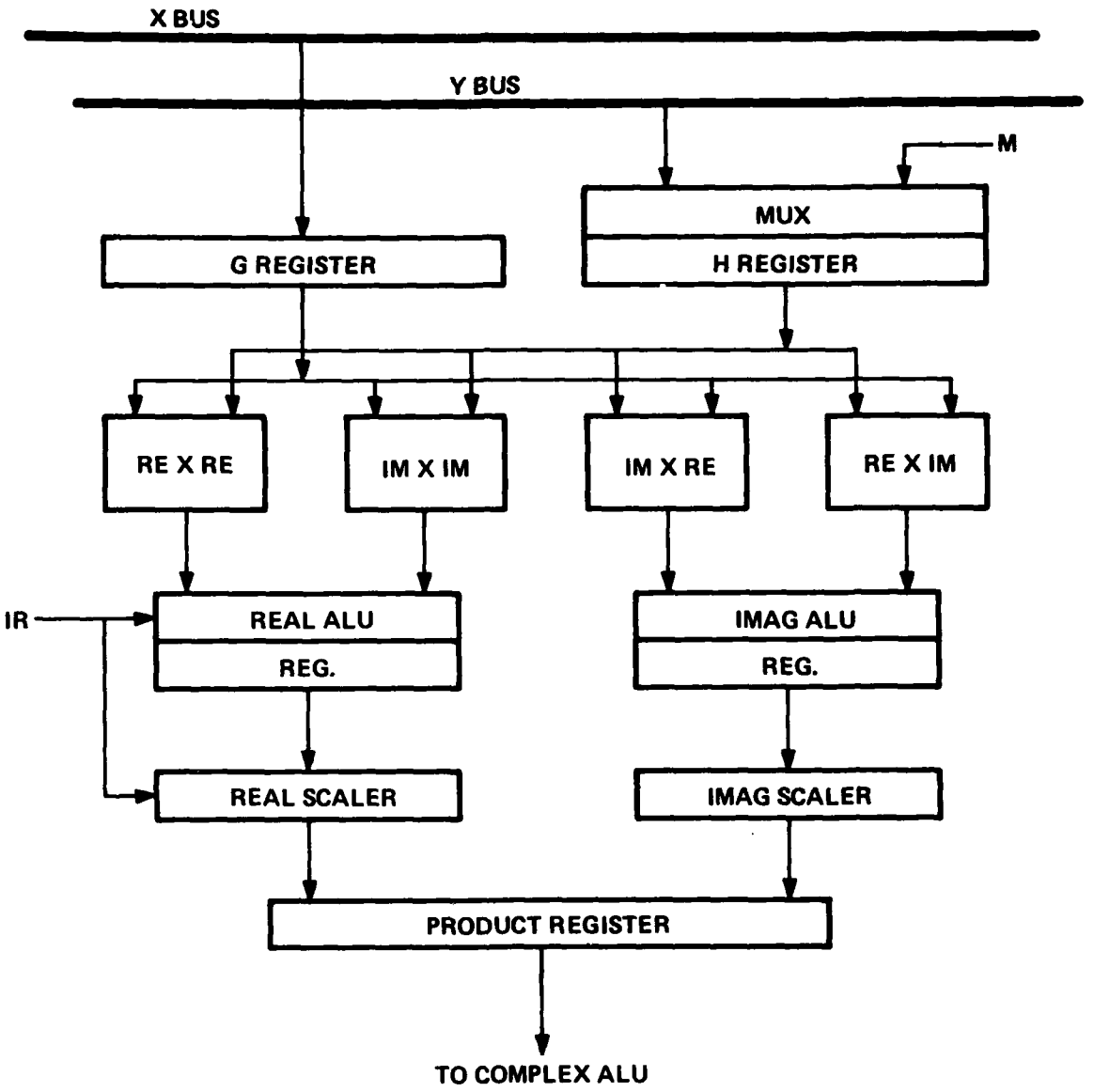
In one machine cycle, the following operations are possible:

- One complex multiply
- One scale operation on the complex product
- One complex add or subtract
- One shift operation on the complex ALU
- Three address calculations
- One read or write for each memory
- One program control operation.

The entire machine is driven by a microprogrammed memory and program control unit which provides cycle-to-cycle control of all elements.

5.2.2 Complex Multiplier

Figure 5-4 shows an expanded block diagram of the Complex Multiplier (CMLY). The multiplier accepts two 32-bit complex numbers and generates a 32-bit complex product each machine cycle with a throughput delay of four cycles. The G input is always sourced from the X bus, while the H input may come from the Y bus or the M register. The complex conjugate of either the G input or the H input may be specified in the instruction set. Following the input registers, four TRW MPY-16HJ multiplier chips are used to generate the four partial products involved in the complex multiplication. The real and imaginary components are summed in separate ALUs. Since a -A-B operation



OPERATIONS

XY	X x Y
XCY	X* x Y
XYC	X x Y*
XM	X x M
XCM	X* x M
XMC	X x M*

3466-80E

Figure 5-4. Complex Multiplier Configuration and Operation

cannot be performed in the ALUs, a multiplication of both G and H conjugated is accomplished by multiplying G times H and making a sign correction of the imaginary part in the complex ALU section of the KSP.

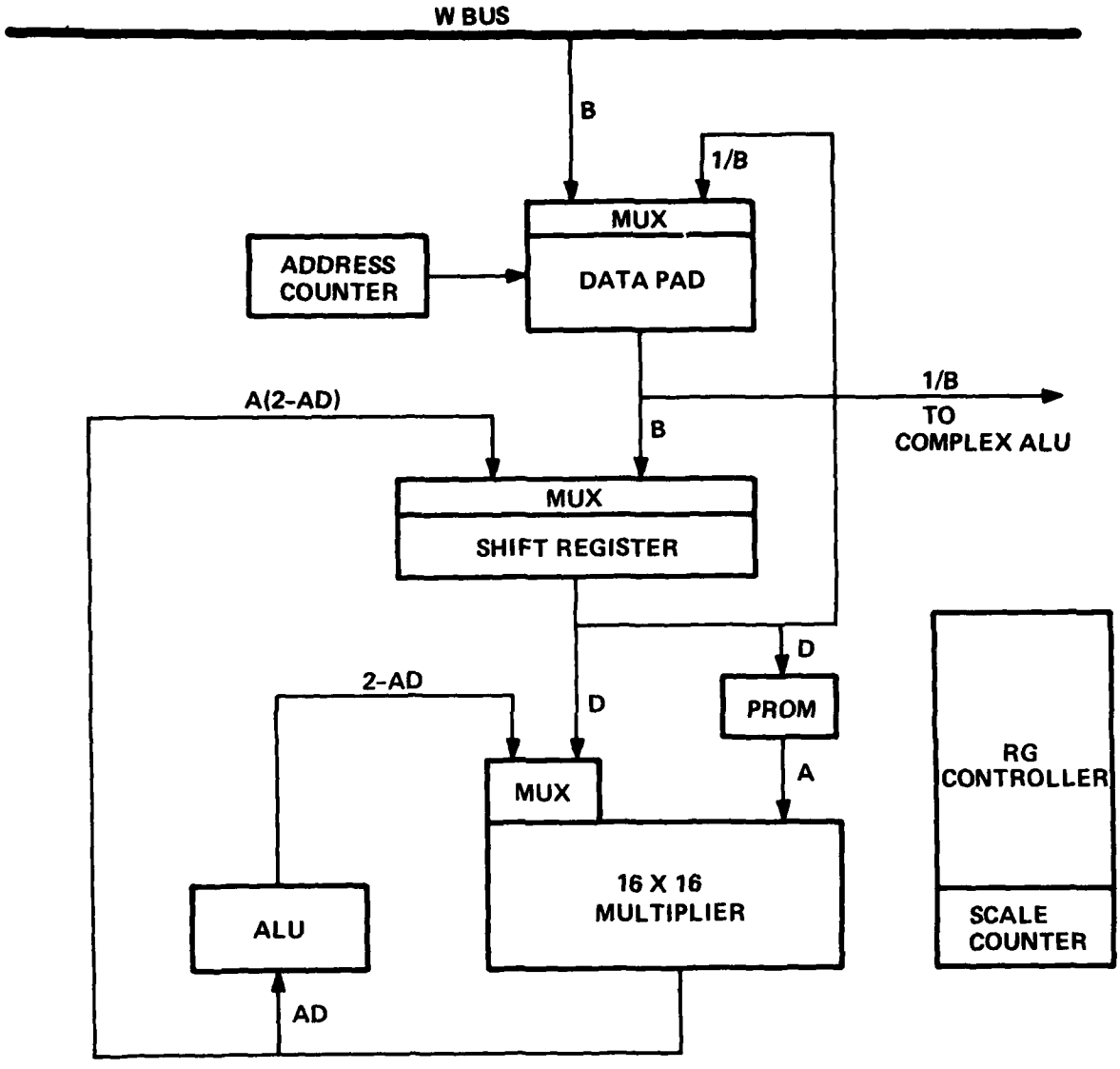
The complex scaler shifts the ALU Register output up to 7 places under program control. This is done in a single cycle, regardless of the number of shifts. Each scaler detects shift dependent overflows, and under such conditions saturates the output to the most negative or positive 16-bit twos complement number. The 32-bit complex product is stored in the Product Register, and is fed directly to the Complex ALU input multiplexer.

5.2.3 Reciprocal Generator

Figure 5-5 shows the Reciprocal Generator (RG) that inverts each element of a real vector with up to 64 elements. Reciprocals are generated using Newton's method with four iterations [22]. The first three iterations are performed by table lookup.

The vector of real scalers, B, is written into the Data Pad under microprogram control. Further operation of the Reciprocal Generator is controlled by a dedicated controller, independent of the main KSP control logic. Independent operation results in an apparent reciprocal computation period of two cycles: one to load and one to unload each operand.

Each value is normalized in the Shift Register and used as the address in a table lookup of the approximate reciprocal, A, accurate to 8 bits. In the two successive machine cycles, the value A(2-AD) is generated, which is the reciprocal of the normalized B, accurate now to 16 bits. This value is returned to the Shift Register where it is scaled by a factor inversely proportional to the factor originally required to normalize B. The reciprocal



INSTRUCTIONS

RGRS	-	RESET
RGLD	-	LOAD
RGST	-	START
RGRD	-	READ

3465-80E

Figure 5-5. Reciprocal Generator Block Diagram

is then written into the Data Pad, overwriting B. When all the values have been reciprocated, control is returned to the main KSP control logic, which reads the reciprocals out of the Data Pad and into the Complex ALU.

Figure 5-6 is an Algorithm State Machine (ASM) diagram of the RG Controller. The machine idles in state 0 waiting for a start command from the KSP program. State 1 normalizes the value B in the Shift Register and loads the multiplier. Scaling of the reciprocal and its storage in the Data Pad occurs in State 6. Before exiting State 6, the Data Pad Address Counter is examined to determine if all the elements in the vector B have been operated on. If so, the RG Run Flag is cleared and the KSP program may read from the Data Pad. If not, the machine returns to state 0 with the Run Flag still set, and the next element of B is accessed.

5.2.4 Address Processors

Calculation of addresses for data memory operands must occur concurrently with other arithmetic operations during execution of the KSP algorithm. Large segments of the algorithm require three addresses every cycle. Most of the address calculations are simple indexed array operations which can be handled by counters. However, the triangular configuration of the U_{NN} and Δ_{NN} matrices require more sophisticated address processors during calculations involving these arrays.

The configuration of the KSP address processors shown in Figure 5-7 satisfies the requirements for address calculations during execution of the Kalman update algorithm. The Memory Address Register (MAR) is loaded from an arithmetic unit with dual input data selectors. An independently controlled counter is used to count or hold any index value to be added or subtracted

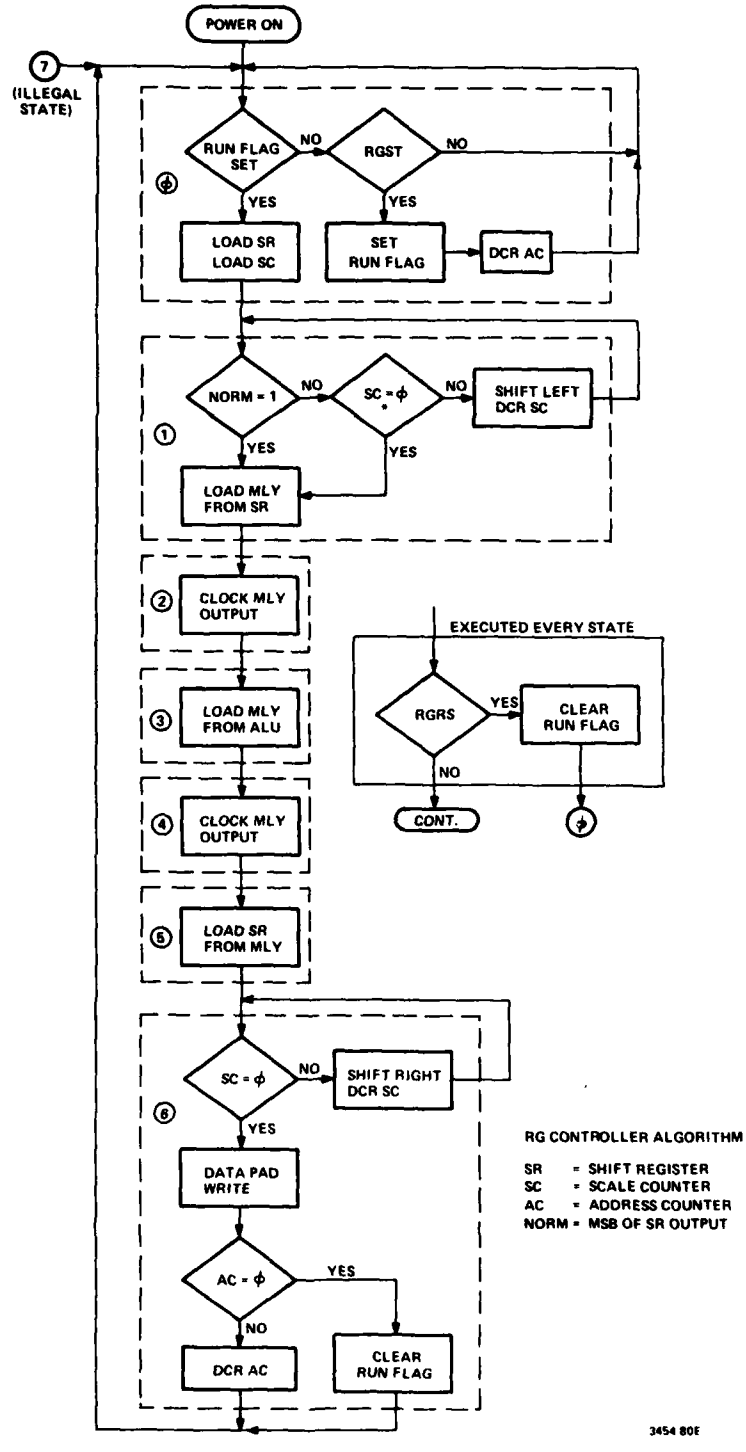
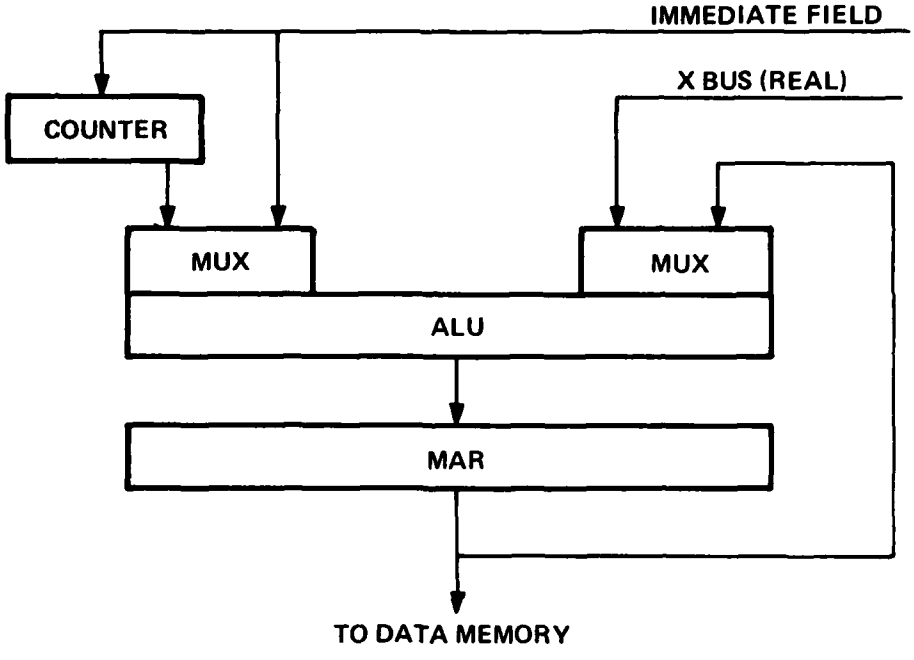


Figure 5-6. RG Controller Algorithm



	MAR OPERATION		COUNTER OPERATION
0	NOP	0	NOP
1	IMMED → MAR	1	IMMED → CTR
2	MAR-1 → MAR	2	CTR + 1 → CTR
3	MAR + 1 → MAR	3	CTR-1 → CTR
4	MAR - CTR → MAR		
5	MAR + CTR → MAR		
6	X BUS → MAR		
7	CTR → MAR		

3464-80E

Figure 5-7. Memory Address Processor Configuration and Operation

from the MAR. The configuration is capable of an add operation and an index operation in one cycle. Immediate address values from the instruction register can be used to preset the MAR or the counter. The MAR may also be loaded from the X bus, thereby providing an indirect address capability.

5.2.5 Microprogram Control

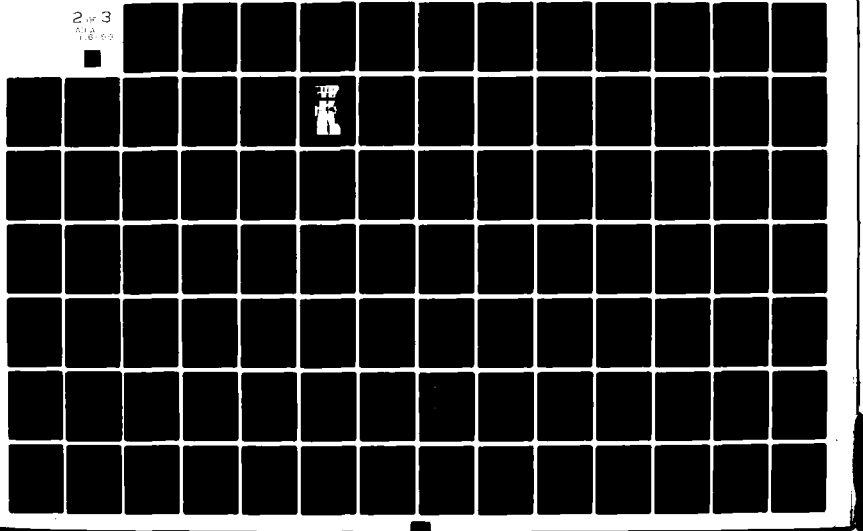
Figure 5-8 shows a block diagram representation of the Microprogram Controller. This section of the KSP generates addresses for the microprogram memory and control signals for the entire machine based on the operand from the Instruction Register. Resources of the controller consists of: a program control element containing a program counter, a four-level program stack, and a full adder; three independently controlled index counters for program iteration and indexing; a configuration register to control Data Memory 2 and 3 instructions.

Operands for the controller are supplied through the I/D Multiplexer. Direct operands come from the Instruction Register, indirect operands from the X Bus. Jump addresses, counter values, and configuration codes represented by operands are transferred through the I/D Multiplexer.

The Configuration Multiplexer and Register are a simple feature of the control architecture that greatly reduce the size of the microprogram for algorithms like the KSP program. By switching various fields of the code from the microprogram memory, the same instruction may be configured differently in the instruction register.

Figure 5-9 shows the 96-bit microprogram instruction word that drives the processor. The word is divided into subfields which provide direct control of the hardware during each machine cycle. The large number of bits in the

AD-A116 859 GTE SYLVANIA INC NEEDHAM HEIGHTS MASS F/G 17/2
HF WIDEBAND MODEM.(U)
APR 82 V ELLINS, P H ANDERSON, M N SANDLER F30602-79-C-0099
UNCLASSIFIED RADC-TR-82-85 NL



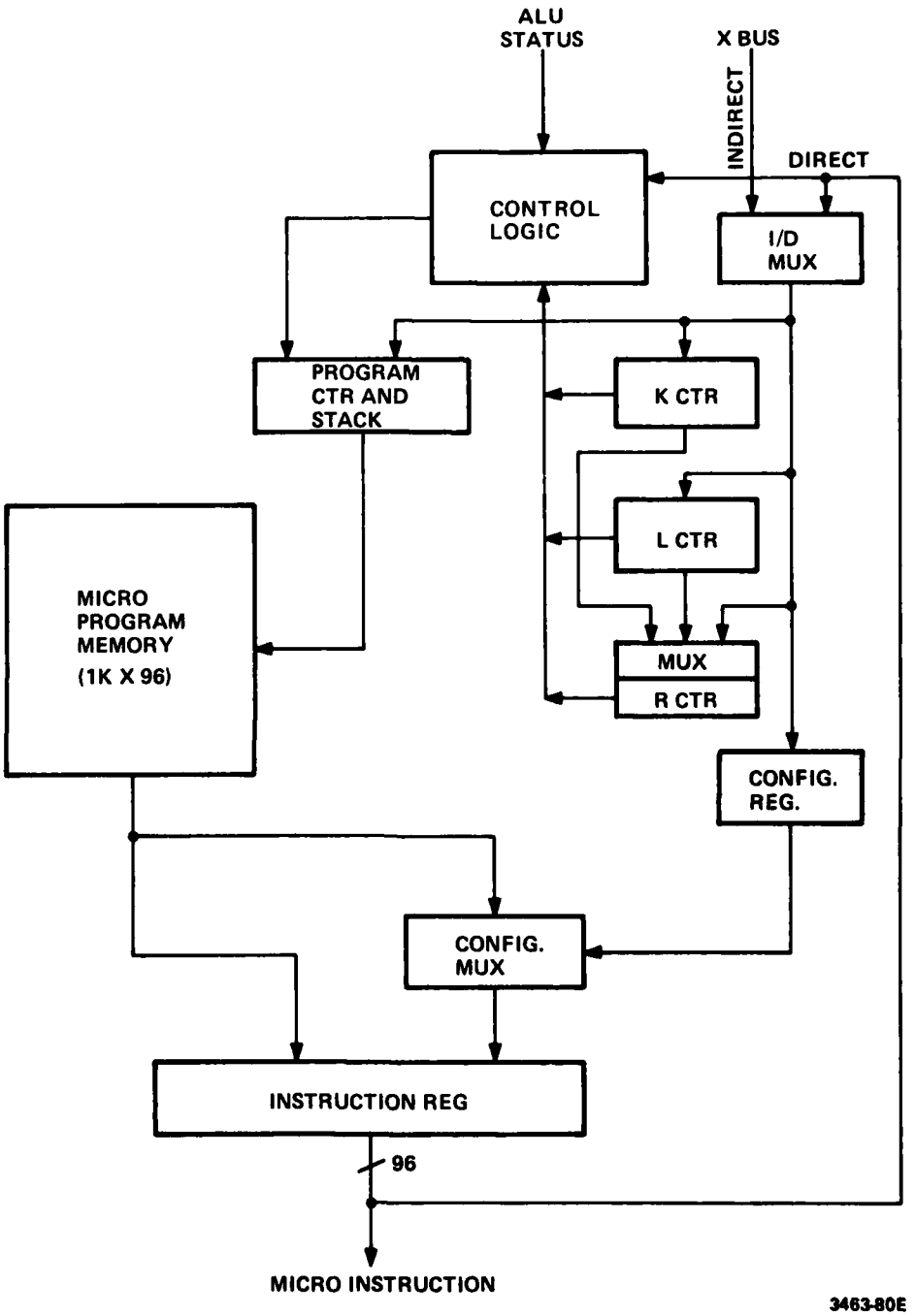


Figure 5-8. Microprogram Control

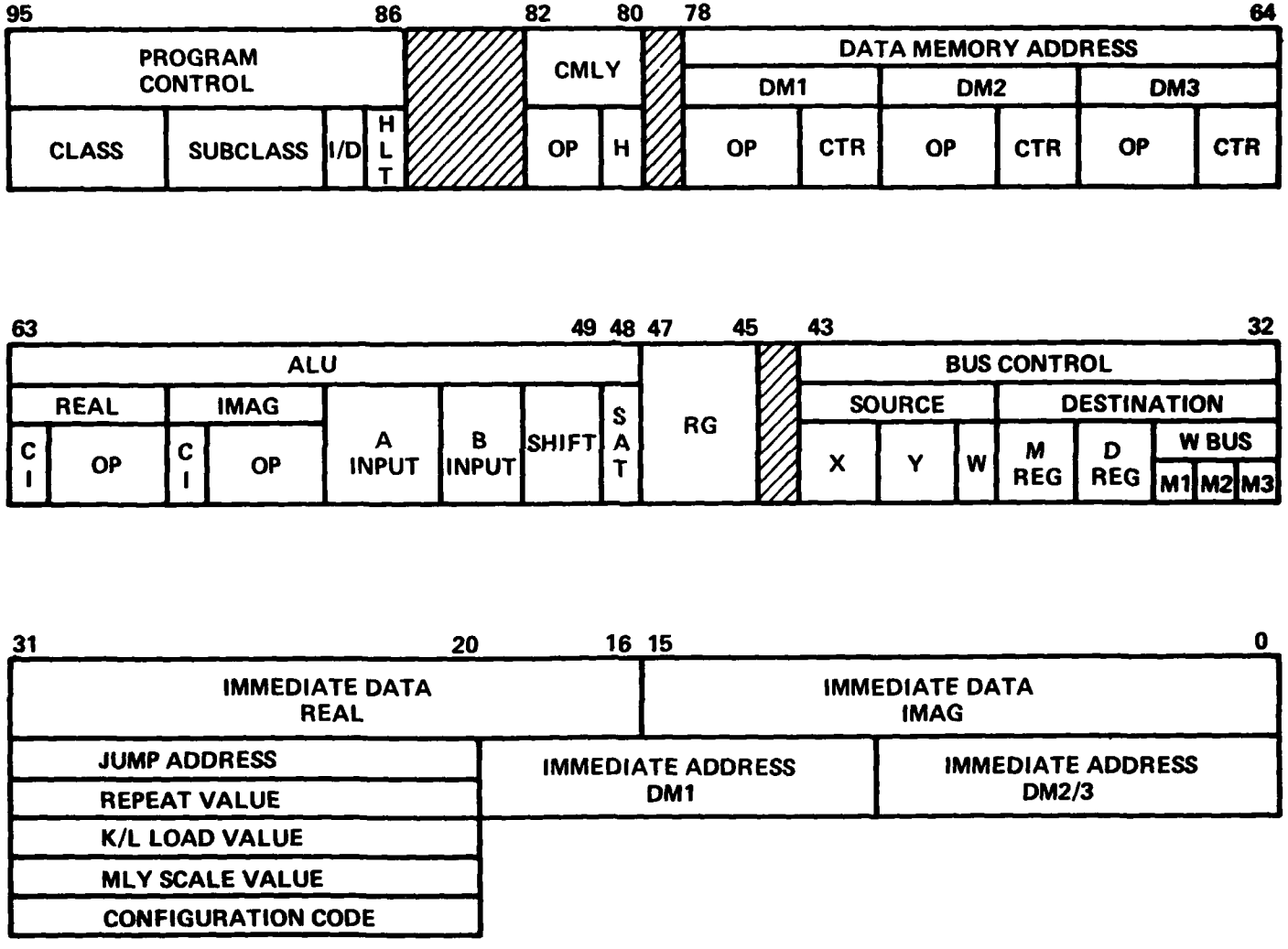


Figure 5-9. KSP Microinstruction Word

instruction word results in reduced hardware complexity and maximum processor performance at the expense of having to account for pipeline effects and parallel operations during software development.

6.0 REAL-TIME SOFTWARE

The real-time software for the HFWBM encompasses approximately 7000 lines of commented Mark IV assembly language code and data table entries. Additional KSP assembly language code was developed to implement the equalizer adaptation algorithm. The KSP code is highly intricate and compact (because of the 56-bit instruction words and parallelism) and will not be described here. The Mark IV software will be briefly described; detailed program listings can be found in the separate *Program Maintenance Manual* [23].

The term real-time "software" describes a transitory stage of the HFWBM system. The delivered equipment contains only "firmware" in which the real-time programs and data tables are permanently "burned" in read-only memory. Thus, the summary contained in this section simply serves to provide an indication of how the routines are organized and what they do. More extensive documentation such as that contained in Ref. [23] may be of use as a reference or permanent record of details; however software "maintenance" is not really applicable in the normal use of that word.

The following describes the functions performed by each of the major routines:

- PWRS - clears data memory, clears I/O lines, initializes interrupt handlers
- LPBK - executes ARQ loopback test
- SLFTST - generates 4 frames of modulator data, then switches to demodulator function
- WAIT - checks flags set by interrupt handlers
- PCAR - generates frames of pure carrier
- ALTDA - generates frames of alternating data

AFDA - generates frames that alternate at the frame rate

TRDT - generates training frame sequence

DATR - transfers actual modem data

SHPF - implements modulator shaping filler

CARMOD - heterodynes up by 1800 Hz

HETRO - heterodynes down by approximately 1800 Hz

SYNFLT - implements symbol synchronizer exclusive of PLL

SYNC - implements synchronizer PLL

KALMAN - implements KSP interface

CARRIER - implements carrier tracking algorithm

INST - implements arc tangent routine

FRSYN - implements frame sync histogram

DETCT - trasfers actual modem data (decoding logic)

DETC - implements mode detectors for acquisition logic

XMTD - executes high data rate transmitter

DMOD - execute high data rate receiver

AQRM - ARQ transmitter

AQDM - ARQ receiver

The top level flow chart given Figure 6-1 shows the organization of these major routines and their relationship in the normal operation of the HFWBM equipment. The interested reader can also refer to Section 3.3.4 for a flow chart of the acquisition process.

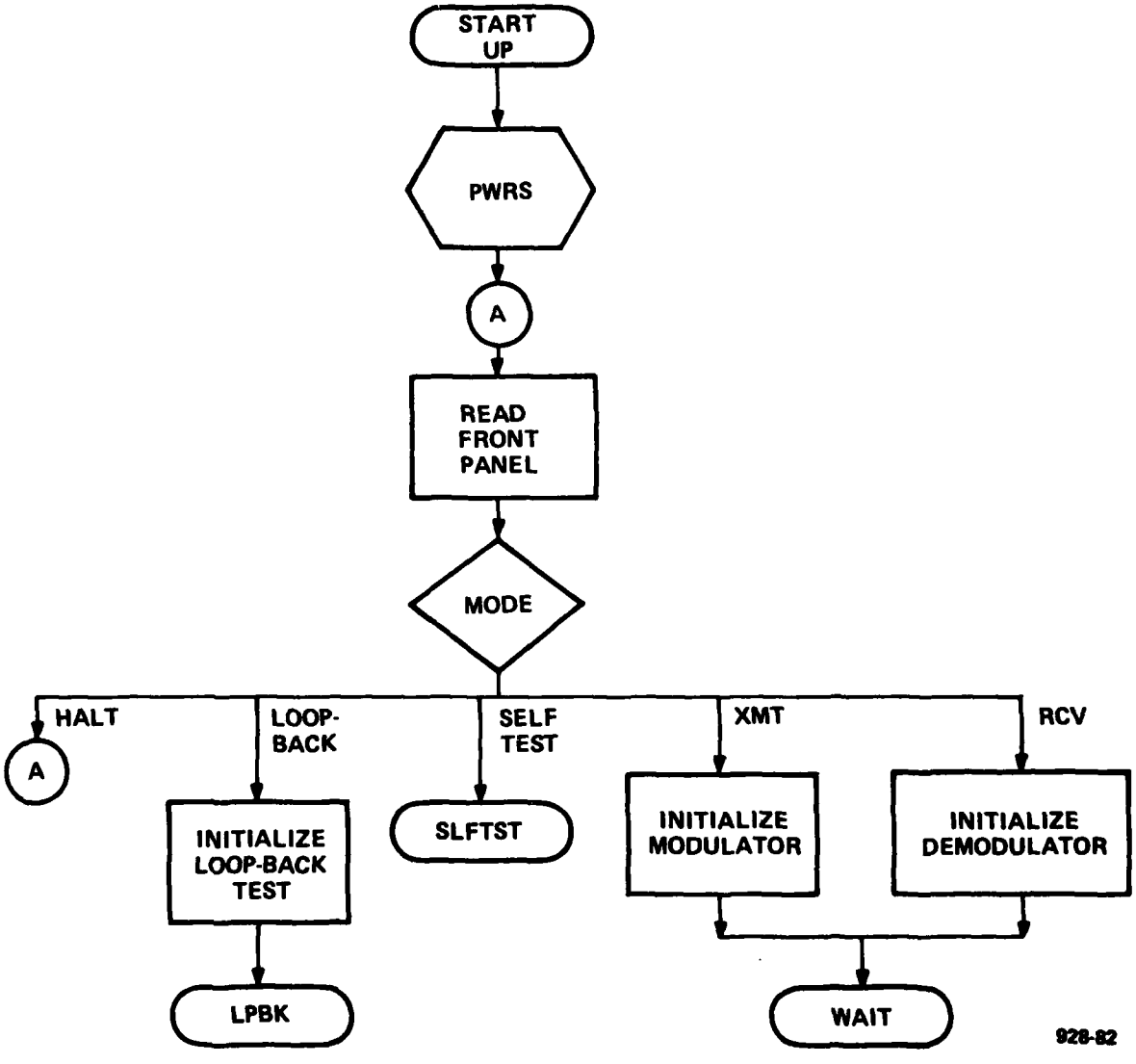


Figure 6-1. Top-level Flow Chart of Real-time Mark IV Software (Sheet 1 of 5)

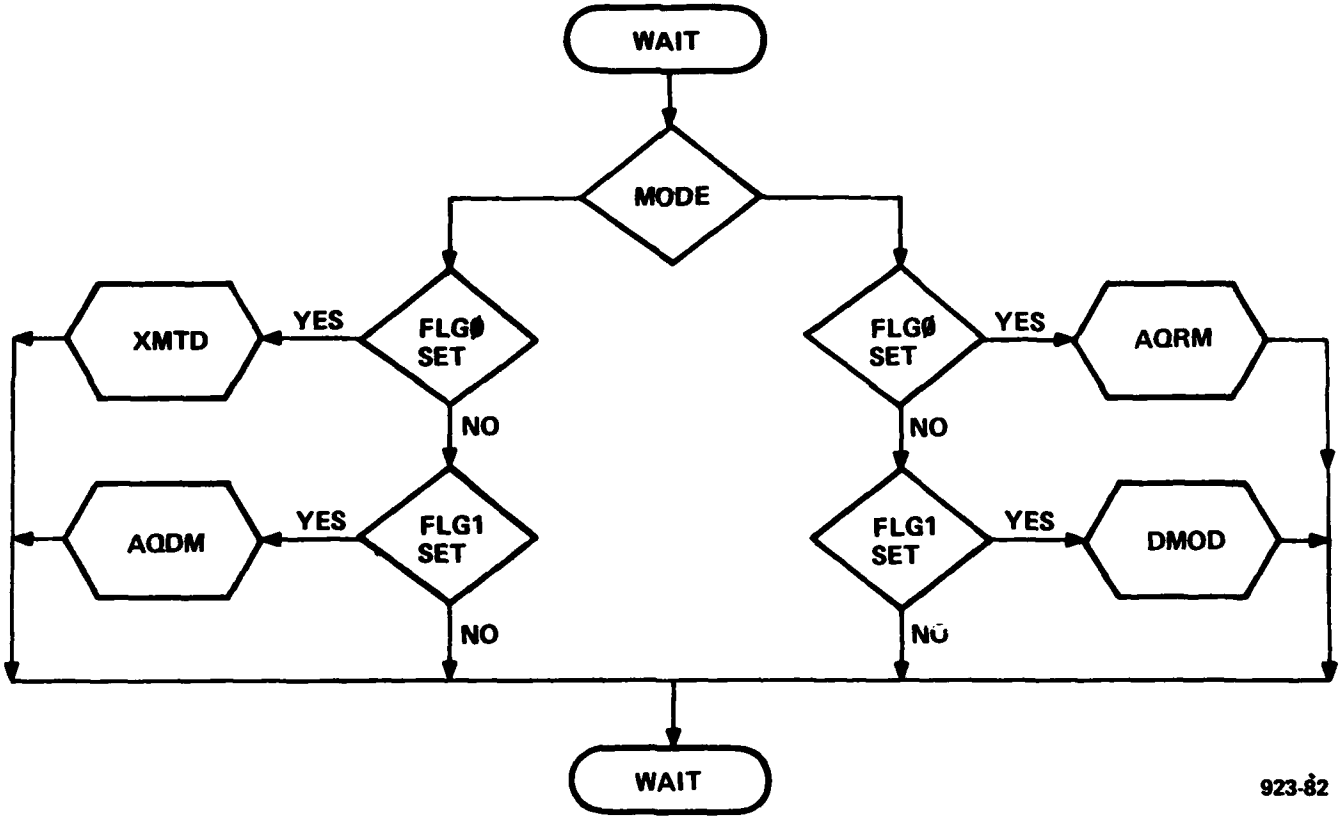


Figure 6-1. Top-level Flow Chart of Real-time Mark IV Software (Sheet 2 of 5)

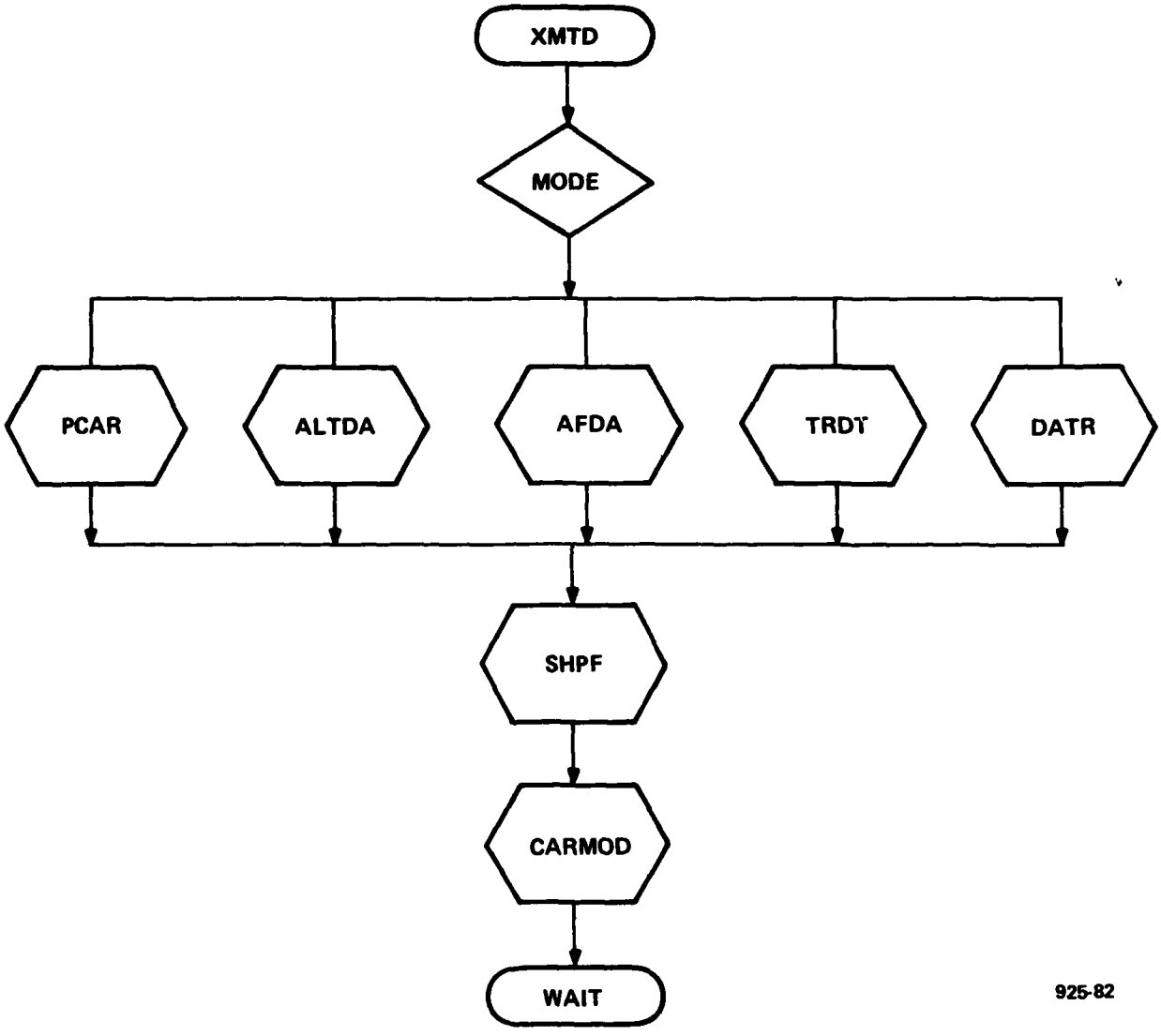


Figure 6-1. Top-level Flow Chart of Real-time Mark IV Software (Sheet 3 of 5)

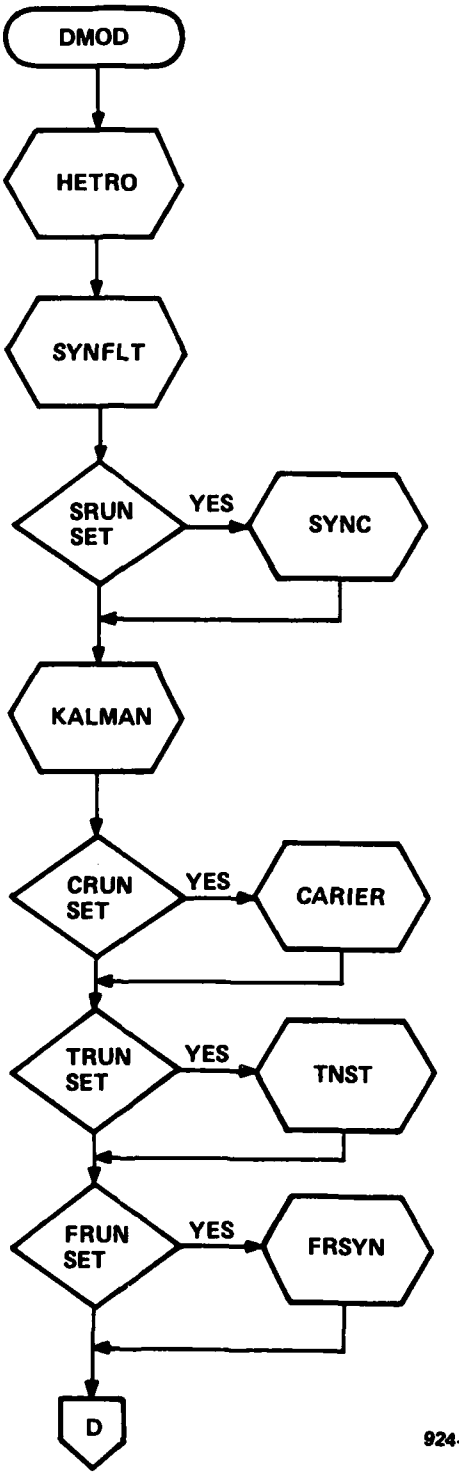


Figure 6-1. Top-level Flow Chart of Real-time Mark IV Software (Sheet 4 of 5)

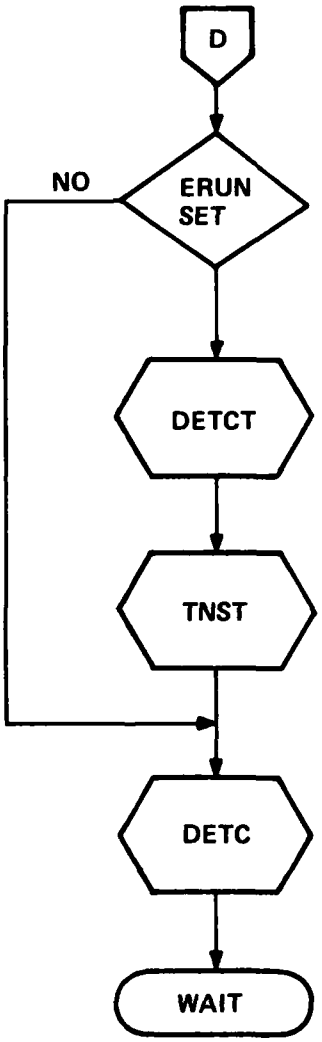


Figure 6-1. Top-level Flow Chart of Real-time Mark IV Software (Sheet 5 of 5)

7.0 SUPPORT SOFTWARE

GTE has independently developed support software on the PDP-11 for both the Mark IV and the High Speed Signal Processor (HSSP) used for the KSP. This software includes a cross assembler, a down loader and a simulator. The Mark IV support software is described in standard Mark IV documents. This section briefly describes the HSSP support software.

7.1 HSSP Cross Assembler and Downloader

The HSSP assembler is a two-pass assembler written in FORTRAN and is modeled after the Mark IV cross assembler. It assembles from the source code the 96-bit instruction words required by the KSP. The first line of source code must be a control line indicating the number of listings and the number of packed binary files (e.g., NL = 1, NB = 1). Pseudo Ops are preceded by a dot (.). Labels are followed by $ (for local symbols) and : (for global symbols). In addition to spaces, the assembler also accepts tabs, making it easier to type attractive listings.

After reading the control card, the assembler will begin execution of Pass 1 and will signify this by typing

PASS 1

At the beginning of Pass 2, it then types

PASS 2

at the conclusion of the assembly, it types

N ERRORS

where N is the number of error lines found by the cross assembler.

Assuming a control line of

NL = 1, NB = 1 (number of listings = 1, number of of binary packed files = 1)

outputs will be a list (.LST) file and a packed binary (.PBJ) file. The .LST file will contain the binary listing of the assembly and the .PBJ file contains the packed binary object file.

The assembly language code for the KSP is written as follows:

LABL$ OPC1, OPC2, ...OPCN JB, ADDR, RA, RB

LABL is the label field and is separated from the operation field by a $ or:. During Pass 1, LABL is assigned the value of the Program Counter (PC) at that location. It is separated from the operation field by a tab or at least one space character.

The .LST file is used by the programmer to debug and alter sourrce code. It lists the diagnostics and the instruction words along with the source code. Figure 7-1 shows a sample .LST output file.

The .PBJ file is the packed binary file and will be downloaded through the Mark IV into the KSP. The downloader support software allows the programmer to enter the .PBJ file into the Mark IV which will then transfer the data to the KSP.

7.2 HSSP Simulator

An HSSP simulator was developed which runs under the RSX-11 Operating System. It is modeled after the Mark IV Simulator and executes the KSP assembly code and performs the logical and arithmetic operations required of the Kalman Processor. This allows for modular debugging of large programs before installation into the final system. Using the simulator, the

```
KSP -1-11 V14
    1:                                  MI.=1,MR=1,M
    2:  0000                                                    NUMS
    3:  0000                                                    BLOCK:
    4:                                          000000015       PARM=21.
    5:  0000  0000 0000 0000 0600 0000 0000     RCLR,S12                                    'CLEAR ALU
    6:  0001  4000 10R0 0000 0600 0CR1 902R     A1LN,A2LN,S12,JMP           200.,100.,50
    7:  0002  C3R6 31R0 0000 0600 01F0 0000     KLD,IND,A1IN,A2IN,XY,S12    30.             'LOAD IND K WITH 30
    8:  0003  D300 10R0 0000 0000 FFFF FFFF     LLD,A1LN,A2LN               4095.,1023.,1023.
    9:                                          00000002A       PARM2=PARM*2.
   10:  0004  D300 0000 0000 0000 02A0 0000     LLD                         PARM2
   11:  0005  0606 31R0 0000 0600 0000 0000     REP,A1IN,A2IN,XY,S12                        'REPEAT 4 TIMES
   12:  0006  R006 31R0 3040 0600 0000 0000     REPK,A1IN,A2IN,XY,RADD,PAMX,ARMX,S12        'ADD ACC WITH P REG,REPEAT M
   13:  0007  0000 1000 3040 064R 0004 0000     A1LN,RADD,PAMX,ARMX,S12,DNX0    400
   14:  000R  7000 1000 106R 0651 0005 0000     RET,A1LN,RRMA,AAMX,DRMX,S12,DNN1    500
   15:  0009  0000 0000 0000 0051 0000 0000     DNN1
   16:                                          .END

 CHECKSUMS                  HEX         OCTAL
    PROGRAM MEMORY SIX= CF92        147622
   PROGRAM MEMORY FIVE= 0580        152600
   PROGRAM MEMORY FOUR= 70ER         70350
  PROGRAM MEMORY THREE= 2AEA         25352
    PROGRAM MEMORY TWO= 1109         10411
    PROGRAM MEMORY ONE= 9027        110047

                                                                                            3488-80E
    0 ERRORS
```

Figure 7-1. Sample Assembler .LST Output File

programmer is able to interrogate memory locations, onboard registers, and ALU operations, and is also able to measure running time through the use of a software run time counter.

8.0 SYSTEM DEVELOPMENT AND INTEGRATION

The HF Wideband Modem contract required the development of two identical high data rate HF modems, including preliminary and final acceptance testing. As stated previously, this development included programming the Mark IV (an existing GTE programmable processor product line), writing microcode for the KSP (a new high-speed signal processor), and integrating the hardware and software into two complete working modems. Section 7 described the software support tools available for this development. This section summarizes how these tools and related hardware were used in the actual modem development and integration. Modifications made to the original design during and after the hardware/software integration phases are identified.

The general system development methodology consisted of the following:

- Hardware design modifications, front panel layout, I/O, AGC design, etc.
- Hardware build and check-out using special purpose diagnostics
- Concurrent software development and test using simulators
- Hardware/software integration and test
- Conversion of final software to "firmware" (in PROM) for stand alone modem operation.

The primary hardware design modifications involved the Mark IV. The clock circuitry was revised using an AM9513 system timing controller chip to generate four separate clock signals required for A/D, D/A, and RS-232 input/output operation in a ARQ environment. A new front panel and appropriate interface circuitry were configured to support the controls and indicators which are unique to the HFWBM. The multiplier card was redesigned,

replacing four 25S05 multipliers with a single TRW MPY-16HJ 16-bit multiplier. The new card is pin compatible with the previous design and provides a 32-bit product two cycles after loading the MPR, rather than eight as with the previous design. A KSP I/O card was added to the Mark IV to provide the necessary decoding logic and line drivers to coordinate DMA transfers between the Mark IV and the KSP. An AGC circuit for the audio input was added. This permits a controllable equal attack and release time AGC to be used in lieu of, or in addition to, the AGC normally provided in HF receivers. A bypass switch was added to the back of the Mark IV so that the HFWBM AGC circuit can be bypassed when desired. Finally, the standard audio input and output low pass filters in the Mark IV were replaced by wider filters to reduce delay distortion to less than 200μs.

Both Mark IV modifications and the KSP were checked out using special purpose diagnostics. These routines were downloaded into read/write RAM in the Mark IV and KSP, as appropriate. A Mark IV test console provided the necessary link to a PDP-11 computer, as well as providing a capability to examine and alter locations in Mark IV memory. A separate KSP debug panel provided the exam/alter capability for the KSP. A block diagram of the system configuration used for hardware checkout and integration is shown in Figure 8-1.

Software development proceeded concurrently with the hardware development using the assemblers and machine simulators described in Section 7. These support tools were used on a real-time software development facility at GTE. This facility is based on a PDP-11/70 computer running in a time-share mode under the RSX-11M operating system. A picture of the facility is shown in Figure 8-2. Significant portions of the application software were developed

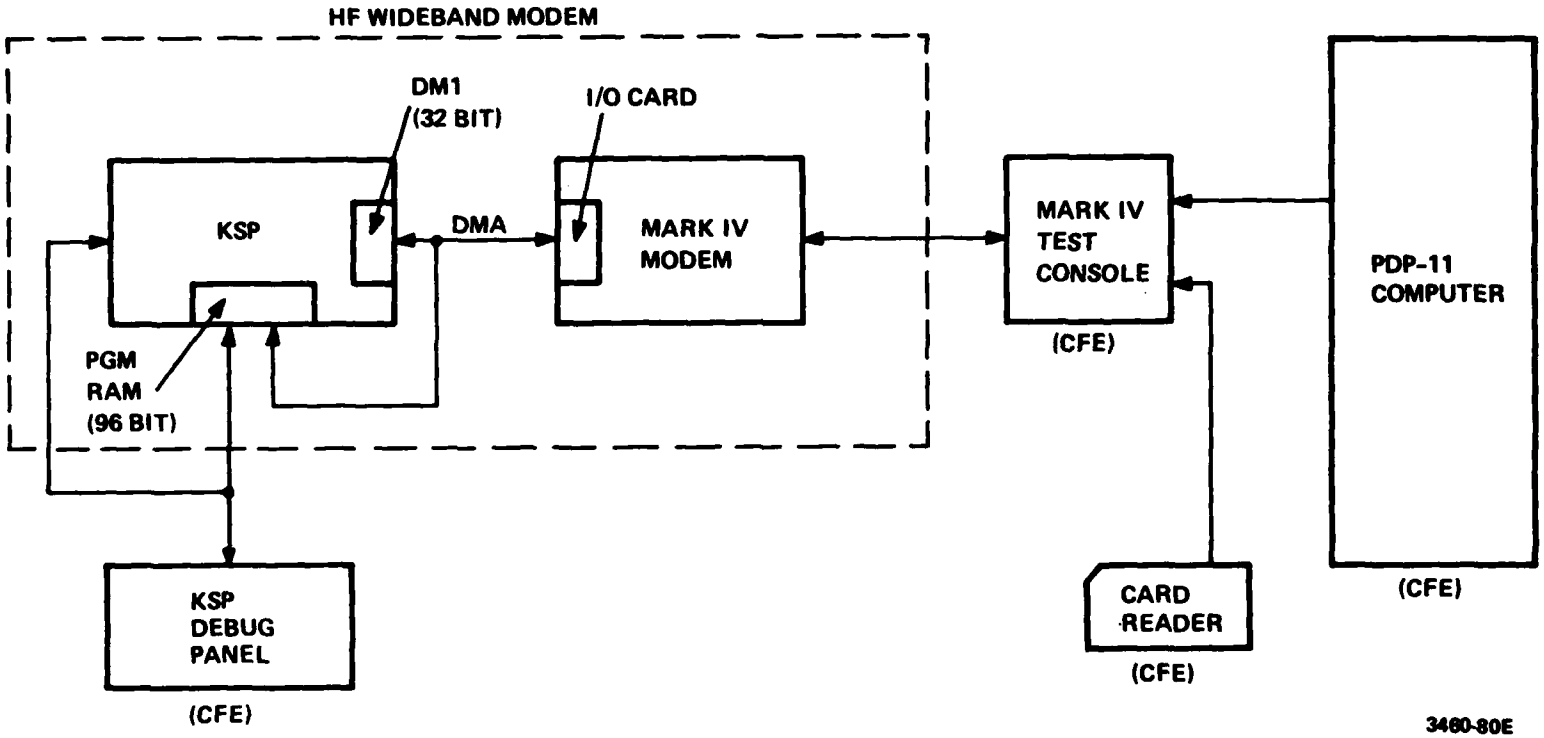


Figure 8-1. HF Wideband Modem Hardware Integration System

Figure 8-2. GTE Real-Time Software Development Facility

and completely debugged using the Mark IV and KSP simulators on the pictured facility. When measurements using the Mark IV simulator run time counter began to show an excessively high processor burden, a decision was made to move a segment of code out of the Mark IV and into the KSP. This code segment corresponds to the demodulator shaping filter which was originally designed for implementation in the Mark IV. Subsequent refinements to the Mark IV software provided the processing margin needed to implement this function, so capacity now exists for it in either machine. In the final implementation it resides in the KSP.

A number of critical software modules could not be debugged on the simulators and were left for hardware/software integration. These modules included the KSP/Mark IV interface software, front panel interface routines, real-time counter control, and all of the two-way logic associated with ARQ operation. A major effort was involved in the successful integration and testing of the complete modem terminal comprising the hardware and final application software. This was accomplished using the two-terminal equipment configuration to be described in Section 9. The operational experience gained in the integration and testing phases led to the adoption of a number of features and parameters as described below.

ARQ Threshold - See Table 8-1 for thumbwheel switch definitions.

Fixed Training - See Table 8-1 for thumbwheel switch definitions.

Displays - See Table 8-2 for rotary switch definitions.

REF DELAY - The calculated beginning synchronization point is placed at the right-most feedforward equalizer tap when the rotary switch is at the +2 position. Counterclockwise rotation of this switch moves the sync point to the left in the equalizer.

TABLE 8-1. THUMBWHEEL SWITCH DEFINITIONS FOR ARQ THRESHOLD AND FIXED TRAINING

Thumbwheel Position	ARQ Threshold	Training Percent
0	-3 dB	0%
1	2	2
2	4	4
3	6	6.25
4	8	8.33
5	10	12.25
6	12	25
7	14	33.33*
8	16	50*
9	18	100

*These values result in a constant clock on the RS-232 interface.

TABLE 8-2. DISPLAY SWITCH DEFINITION

Switch Position	LED Display
TOTAL	
ERR	Total No. ARQ's (NQ)
SYM	Total No. received frames
DATA	
SYM	Total No. accepted info. frames
ERR	Symbol error count (SE)*
A	MSE in equalizer output (NVAR)
B	Selectable debug data

*Internal error rate test only.

Some additional debug features were left in the final software; however, the description of their use is beyond the scope intended for this report. A complete operation and maintenance (O&M) manual was not part of the current contract. Nevertheless, there has been a conscious attempt to provide sufficient data here to permit use of the HFWDM equipment in all of its normal modes of operation.

The final software was burned into read-only program memory (PROM) and read-only data memory (ROM). These memories have been substituted for the read/write random access memory (RAM) in both Mark IVs and KSPs, making the delivered equipment two completely self-contained modem terminals. These terminals need only be powered up with appropriate user cable connections in place for proper modem operation.

The delivered modem terminals have been subjected to GTE's final quality assurance. A complete drawing set was released internally for custody by the Communication Systems Division central engineering files. A similar release of all project software has been made to the Division software control center. This assures the data will be available if future needs require it. It is also a simple matter to replace the read-only memory in the delivered equipment with RAM to restore it to a configuration which operates with true "software" with all of its attendant flexibility.

9.0 FACTORY TESTING

Preliminary acceptance tests were performed at GTE on 22-23 July 1981. These nonfading tests were conducted in accordance with procedures formalized in a document submitted in advance to RADC [24]. This section summarizes the test procedures and presents the test results.

Figure 9-1 shows the equipment configuration for the Factory Acceptance Tests. The spectrum analyzer was used to verify the required 3 kHz spectral occupancy of the transmitted signal. The oscilloscope and RMS voltmeter were used to demonstrate a peak-to-average ratio of under 3 dB, in accordance with the contract specifications. In a dynamic range test, the input signal to the HFWBM demodulator was varied over a 40 dB range. With the AGC enabled, the equalizer output SNR was found to remain above 25 dB for input levels between 0 and -40 dBm. With the AGC disabled, the output SNR remains above 25 dB over the more limited input range of 0 to -9 dBm.

The summing amplifier was used to add noise to the signal prior to the HFWBM demodulator as shown in Figure 9-1. The RMS voltmeter was used to measure the signal-to-noise ratio. A Model 1300 IDS Modem Test Set was used to supply a 2047-bit pseudorandom data pattern and to count errors for the bit-error rate versus SNR curves.

Error-rate measurements were made for 7 tap and 35 tap equalizers. The following T and T/2 spaced configurations were used: T(4,3), T(18,17), T/2(5,2) and T/2(24,11). All measurements were repeated twice, with the HFWBM terminals operated first in one direction and then reversed. The results for 4800, 7200 and 9600 b/s are shown in Figure 9-2 and 9-3. The solid lines in Figure 9-2 represent the theoretical performance for M-ary PSK (with

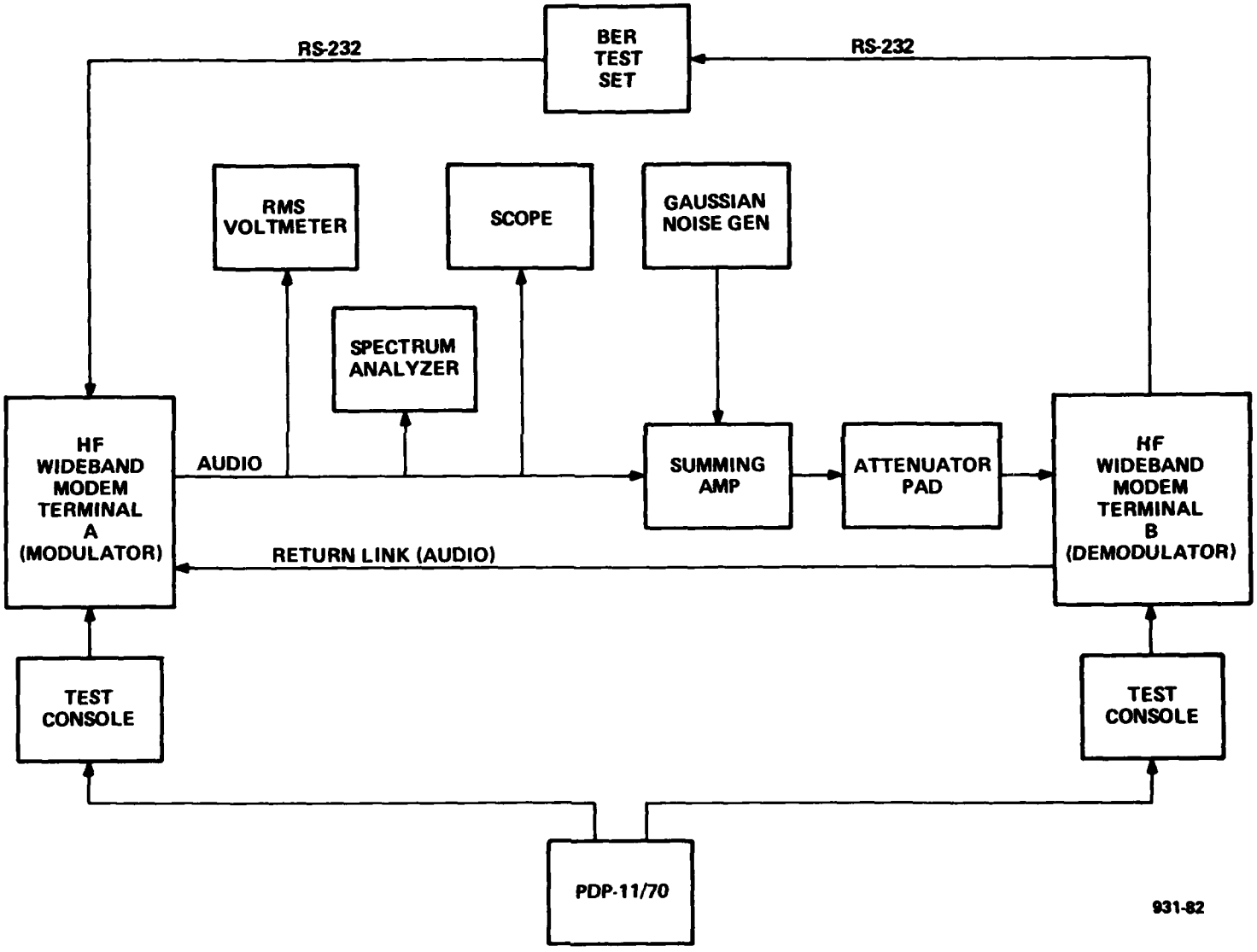


Figure 9-1. Equipment Configuration for Factory Tests

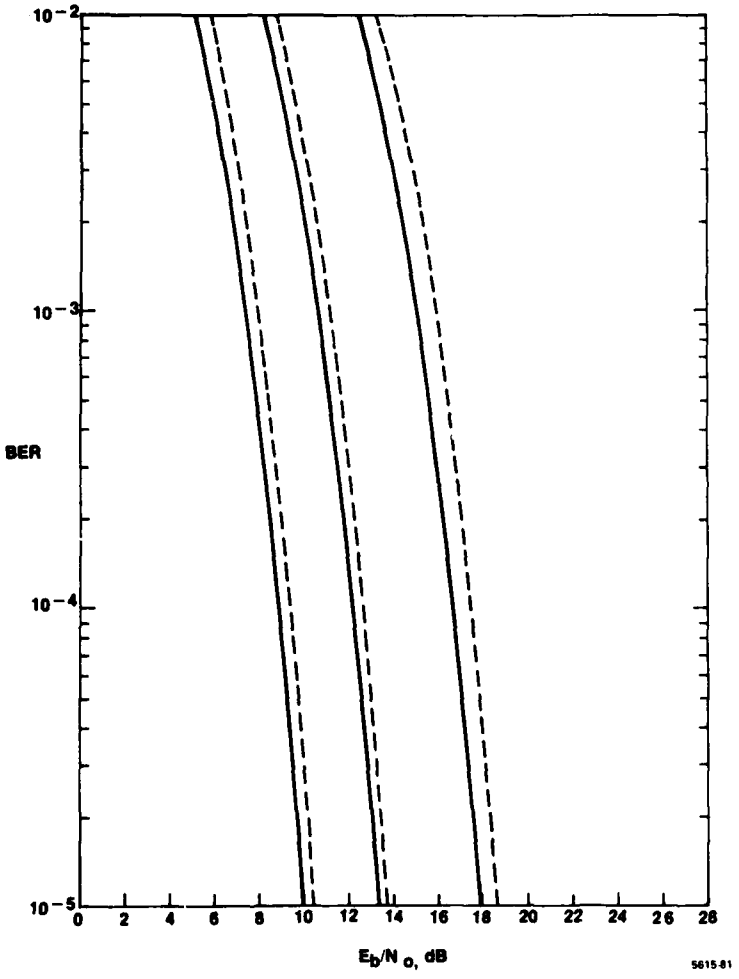


Figure 9-2. Bit Error Rate Versus Signal-to-Noise Ratio per Bit for HFWBM in Gaussian Noise, 7 Tap Equalizers

differential encoding) in Gaussian noise. The dashed lines in Figure 9-2 show the measured HFWBM performance for both T and T/2 spaced 7-tap equalizers. There was no discernable difference in the performance of T and T/2 spaced equalizers in these nonfading tests. The measured results are observed to lie within 1 dB of the theoretical curve, well within the contract specification. The effects of using too long an equalizer are shown in Figure 9-3 which displays the corresponding results for the 35-tap (T and T/2) equalizers. Since there was no discrete (channel) multipath in these tests, the equalizer needs only to be long enough to span the dispersion introduced by the HFWBM analog anti-aliasing filters. Seven taps are adequate. Going to a significantly longer size can actually degrade performance due to self-noise introduced by unneeded taps. Comparing Figure 9-2 and 9-3, the amount of degradation introduced at the full 35-tap capacity of the HFWBM is about 2 dB. These results suggest that it will generally be fruitful to adjust the size of the equalizer (as can be done on the HFWBM front panel) to accommodate just the expected or measured total channel dispersion.

The measured performance for 7-tap T and T/2 equalizers and 2400 b/s signaling is shown in Figure 9-4. The measured data at low SNR values was taken using 4-8 percent training. This was found necessary because 100 percent decision-directed adaptation below a symbol SNR value of about 10 dB tended to break down. In particular, at low SNR values the DFE structure drifts into a state where the feedforward tap coefficients are all very small (or zero) and the feedback coefficients assume values which produce an equalizer output sequence whose elements all lie on points of the desired signal constellation. In this situation, the equalizer feedback section has become, in effect, a linear recursive sequence generator, and the state is

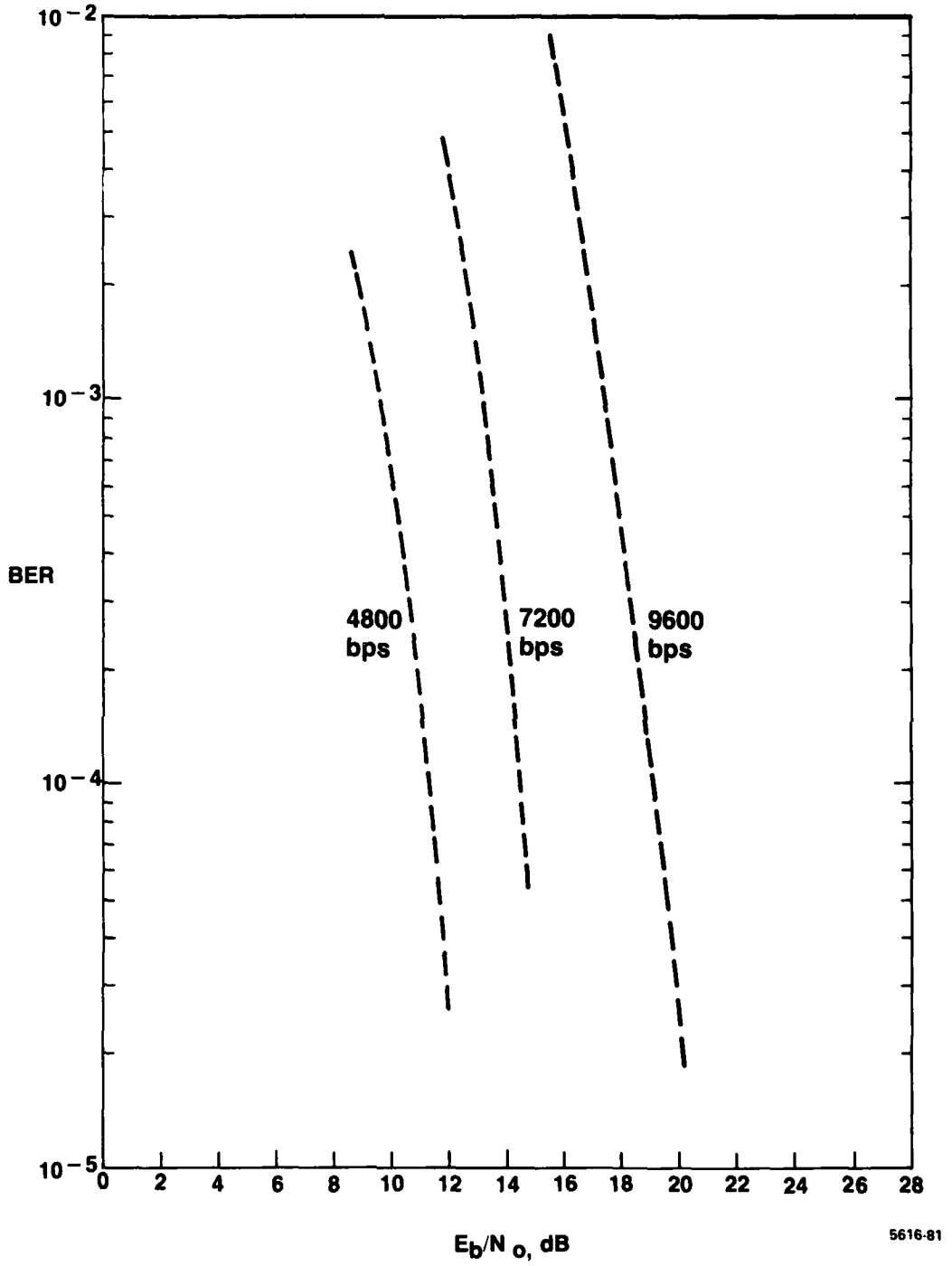


Figure 9-3. Bit Error Rate Versus Signal-to-Noise Ratio Per Bit for HFWBM in Gaussian Noise, 35 Tap Equalizers

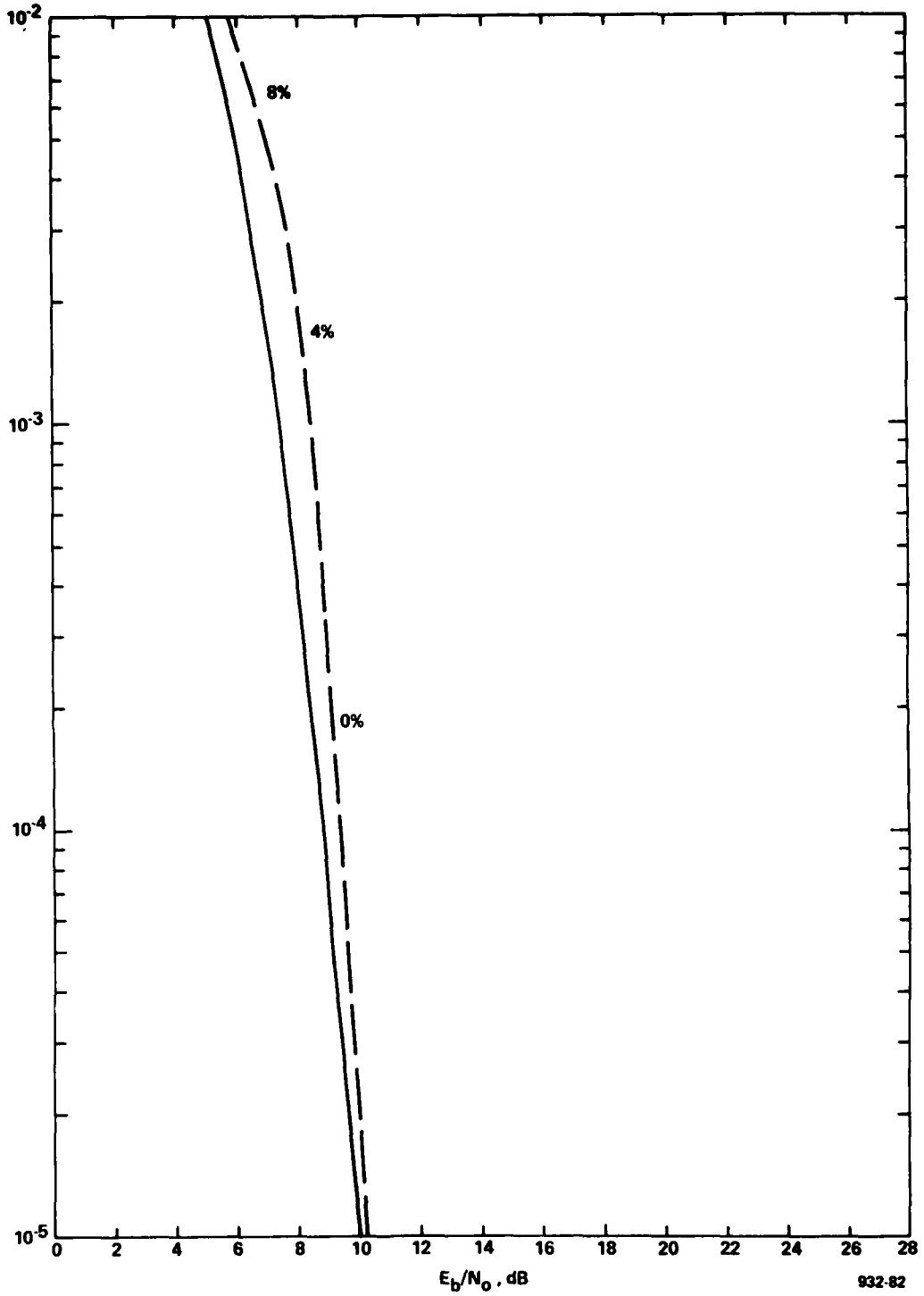


Figure 9-4. Bit Error Rate Versus Signal-to-Noise Ratio for HFWBM at 2400 b/s of the Equalizers

termed "equalizer hang-up" since it will not recover as long as the equalizer stays in the decision directed mode. The use of some (known) training symbols represents a simple and effective way of overcoming equalizer hang-up. The measured results for 2400 b/s are observed to lie within 1 dB of the theoretical curve.

10.0 DICEF TESTS

Final acceptance tests were performed using the real-time HF channel simulator at the RADC DICEF facility over the period September 3-9, 1981. Additional on-the-air tests were accomplished using a 24 km HF link from Ava, N.Y., to Rome, N.Y., on September 10, 1981. This section summarizes the procedures used to conduct these tests and presents the results in graphical form. A brief interpretive discussion is provided as an aid to evaluating the significance of the test results.

10.1 Test Procedures

The final acceptance tests were conducted in accordance with detailed procedures formalized in a document submitted in advanced to RADC [25]. The subsections which follow summarize the test conditions and describe the data collection and data reduction techniques used for the results presented in Section 10.2.

10.1.1 Equipment Configuration

The two HFWBM terminals brought to DICEF were configured with volatile read/write program memory. Accordingly, the real-time modem software was initially downloaded into program memory (from binary files supplied by GTE on an RK05 disk) using the DICEF PDP-11/40 computer. GTE also supplied a DR-11C card and two Mark IV test consoles to effect this computer-to-modem interface. Once the real-time software was downloaded, the connection to the PDP-11/40 was removed and the HFWBM units were operated as stand-alone modem terminals. The PDP-11/40 LA-30 Dec-writer then served as the keyboard interface to the DICEF real-time HF media simulator.

An IDS Model 1300 Modem Test Set was used to supply a pseudorandom serial bit stream to one HFWBM acting as a modulator (Terminal A), and to receive the serial bit stream from a second HFWBM acting as a demodulator (Terminal B). These digital signals, together with clock and status lines, were communicated over an RS-232C interface. The audio output signal from Terminal A was applied (600-ohm balanced) as input to the HF media simulator, and the (600-ohm balanced) audio output of the simulator served as the audio input for Terminal B. A direct cable connection from the Terminal B audio output to the Terminal A audio input established a return link for the ARQ protocol. A strip chart recorder was used to monitor the internal AGC voltage developed at Terminal B. Figure 10-1 illustrates the complete equipment configuration for the DICEF tests.

Since both HFWBM units were designed to be identical, one was arbitrarily selected to serve as Terminal A and the other as Terminal B. A subset of the DICEF tests was repeated with the equipment configured in the reverse direction to verify correct operation of both units as modulator and demodulator.

10.1.2 Test Conditions

The primary purpose of DICEF testing was to obtain results which characterize the error-rate versus SNR performance of the HFWBM operating over a variety of fading channel conditions. Accordingly, four possible multipath distributions were selected for use in combination with eight possible fading situations [25]. For descriptive purposes, the particular multipath structures are identified by a numerical code as shown in Table 10-1, and the fading dynamics are identified by a letter code as shown in Table 10-2. In Table 10-2, the term "Doppler Spread" refers to the RMS bandwidth of the

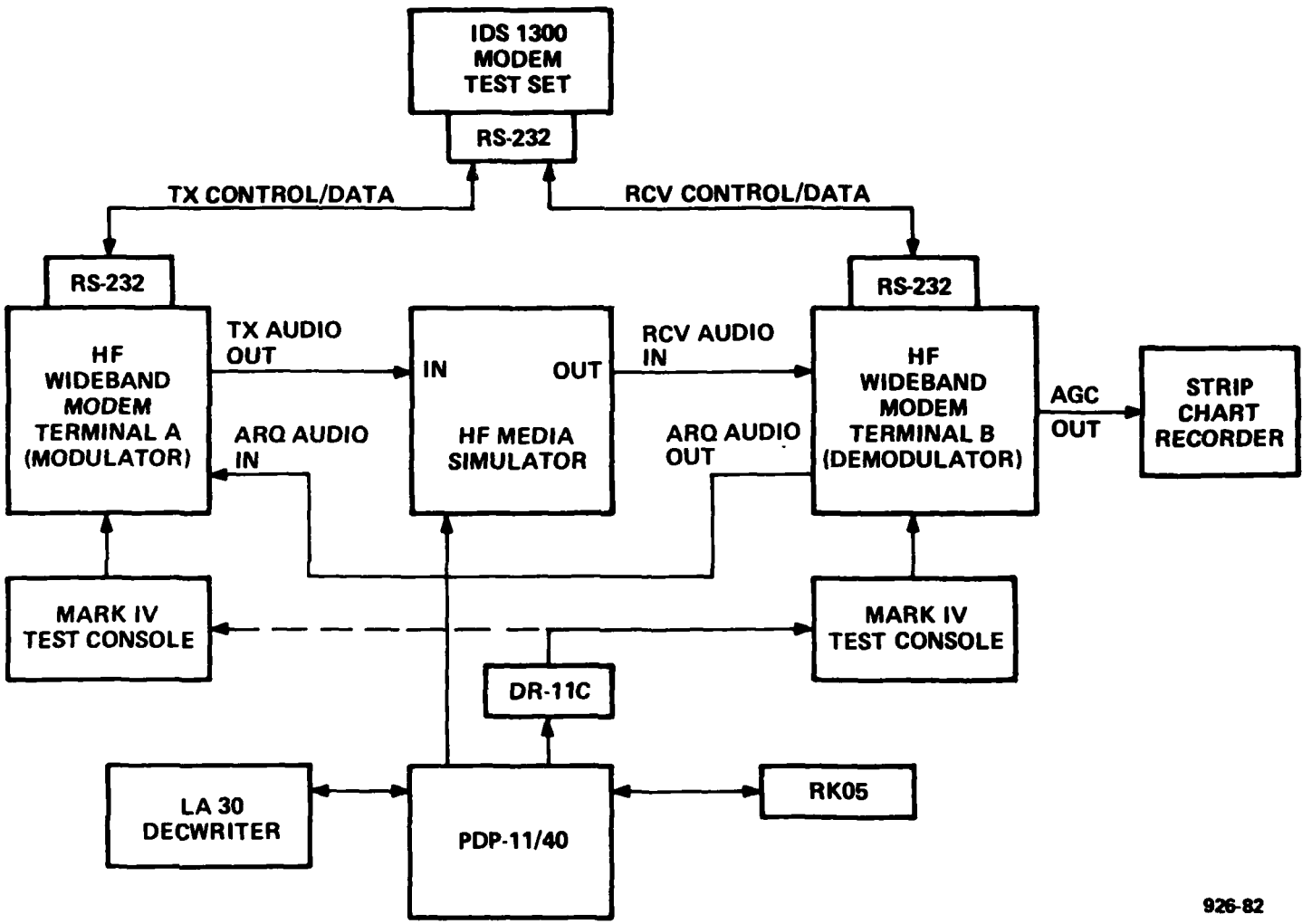


Figure 10-1. Equipment Configuration for DICEF Testing

TABLE 10-1. DISCRETE CHANNEL MULTIPATH CHARACTERISTICS

Channel Identifier	Relative Power (dBm)	Relative Delay (ms)
1	0	0.0
2	-3 -3	0.0 0.4
3	-16 0	0.0 1.2
4	-14 0 -2	0.0 0.6 2.8
5	0 -10	0.0 5.0

TABLE 10-2. FADING PARAMETERS

Fading Identifier	Doppler Spread (Hz)	Differential Doppler (Hz)
A	.05	0.0
B	.05	0.5
C	.05	1.0
D	.05	2.0
E	.10	0.0
F	.10	0.5
G	.10	1.0
H	.10	2.0

Rayleigh fading process associated with each path. All paths used the same Doppler spread. Only one magnetoionic component per path was used. The term "Differential Doppler" in Table 10-2 refers to the difference in mean Doppler shift between the paths. This difference was evenly split into a negative frequency shift on the earliest path and a positive shift on the latest path. (In the case of 3 paths, the middle path had zero shift.)

The modem was operated at data rates of 2400, 4800, 7200 and 9600 b/s. The equalizer was configured with either T or T/2 spaced feedforward taps, with the number of taps selected to span a time interval somewhat larger than the expected multipath spread. The AGC was enabled with the slew rate in the slowest position. Tests were primarily conducted in the ARQ mode with a threshold of 10 dB for 2400-4800 b/s, and 12 dB for 7200-9600 b/s. Some data was also collected in a fixed training mode, where the percent training was varied from 12.5 to 50 percent.

Table 10-3 lists 34 different combinations of channel conditions and HFWBM settings that were included in the formal test plan. For each combination listed, error-rate measurements were taken at a number of SNR values in a range from 12 to 28 dB (E_b/N_o), so that an error rate versus SNR characteristic could be established. An (S) following the curve number in Table 10-3 indicates that, in addition to this series of error rate measurements, a spot check was made at one SNR value with the modem operated in the reverse direction. The fade rate listed in the third column of Table 10-3 represents the composite RMS fading bandwidth of the channel in Hz as computed by the HF media simulator program. The notation T/2(n,m) or T(n,m) is used in the fourth column of Table 10-3 to indicate either a T/2 or T spaced DFE configuration with n feedforward and m feedback taps. The spacing

TABLE 10-3. ERROR RATE CURVES

Curve No.	Channel Code	Fade Rate	Equalizer Spacing	Data Rate	ARQ dB or %
1	1A	0.0500	T/2(8,3)	4800	10 dB
2(S)	1E	0.1000	T/2(8,3)	4800	10 dB
3	2A	0.0500	T/2(8,3)	4800	10 dB
4	2B	0.0503	T/2(8,3)	4800	10 dB
5	2C	1.0010	T/2(8,3)	4800	10 dB
6	2C	1.0010	T(4,3)	4800	10 dB
7	2D	2.0010	T/2(8,3)	4800	10 dB
8	2E	0.1000	T/2(8,3)	4800	10 dB
9	2G	1.0050	T/2(8,3)	4800	10 dB
10(S)	3C	0.3132	T/2(14,6)	2400	10 dB
11	3C	0.3132	T/2(14,6)	4800	8 dB
12	3C	0.3132	T/2(14,6)	4800	10 dB
13(S)	3C	0.3132	T(7,6)	4800	10 dB
14	3C	0.3132	T/2(14,6)	4800	12 dB
15	3C	0.3132	T/2(14,6)	7200	12 dB
16	3C	0.3132	T/2(14,6)	9600	14 dB
17	3C	0.3132	T/2(14,6)	4800	12.5 %
18	3C	0.3132	T/2(14,6)	4800	25.0 %
19(S)	3C	0.3132	T/2(14,6)	4800	50.0 %
20	3D	0.6204	T/2(14,6)	4800	10 dB
21	3H	0.6265	T/2(14,6)	4800	10 dB
22	4C	0.5280	T/2(22,10)	2400	10 dB
23	4C	0.5280	T/2(22,10)	4800	10 dB
24	4C	0.5280	T(11,10)	4800	10 dB
25(S)	4C	0.5280	T/2(22,10)	7200	12 dB
26(S)	4C	0.5280	T/2(22,10)	9600	12 dB
27	4D	1.0520	T/2(22,10)	4800	10 dB
28	4H	1.0560	T/2(22,10)	4800	10 dB
29(S)	5C	0.5771	T(16,15)	4800	10 dB
30	5D	1.1510	T(16,15)	4800	10 dB
31	5E	0.1000	T(16,15)	4800	10 dB
32	5F	0.3044	T(16,15)	4800	10 dB
33	5G	0.5836	T(16,15)	4800	10 dB
34	5H	1.1540	T(16,15)	4800	10 dB

refers to the delay separation between the feedforward taps. The feedback taps are always separated by the symbol interval T.

The 2047-bit pseudorandom data pattern from the IDS Modem Test Set was used for all curves except Nos. 17-19. Because of the high error rates associated with the latter curves, it was found more convenient to use the HFWBM internal error rate test pattern. This avoids the problems of overflow in the error count display on the IDS Test Set. In all cases, the test durations spanned a period corresponding to at least one million information bits. A few much longer tests were made to verify the validity of the error rate measurements.

10.1.3 Data Collection

The following data were recorded during the tests with the HF media simulator:

- AGC voltage versus time
- Channel conditions
- Modem settings
- Information bit error counts (BE)
- Information bit count (NB)
- Total received symbol count (RS)
- Output information symbol count (NS)
- Total ARQ count (NQ)
- ARQ retry count (NR)
- Information symbol error count (SE)

The AGC voltage versus time was recorded on the strip chart recorder for each distinct channel (but not at every SNR value). All strip chart recordings used a chart speed of 10 s/cm and a sensitivity of 0.2 v/cm. Some typical recordings are shown in Figure 10-2. The HF media simulator channel conditions were set up through the LA30 terminal, and a hard copy of this dialog was retained. These conditions were also hand-recorded on a separate

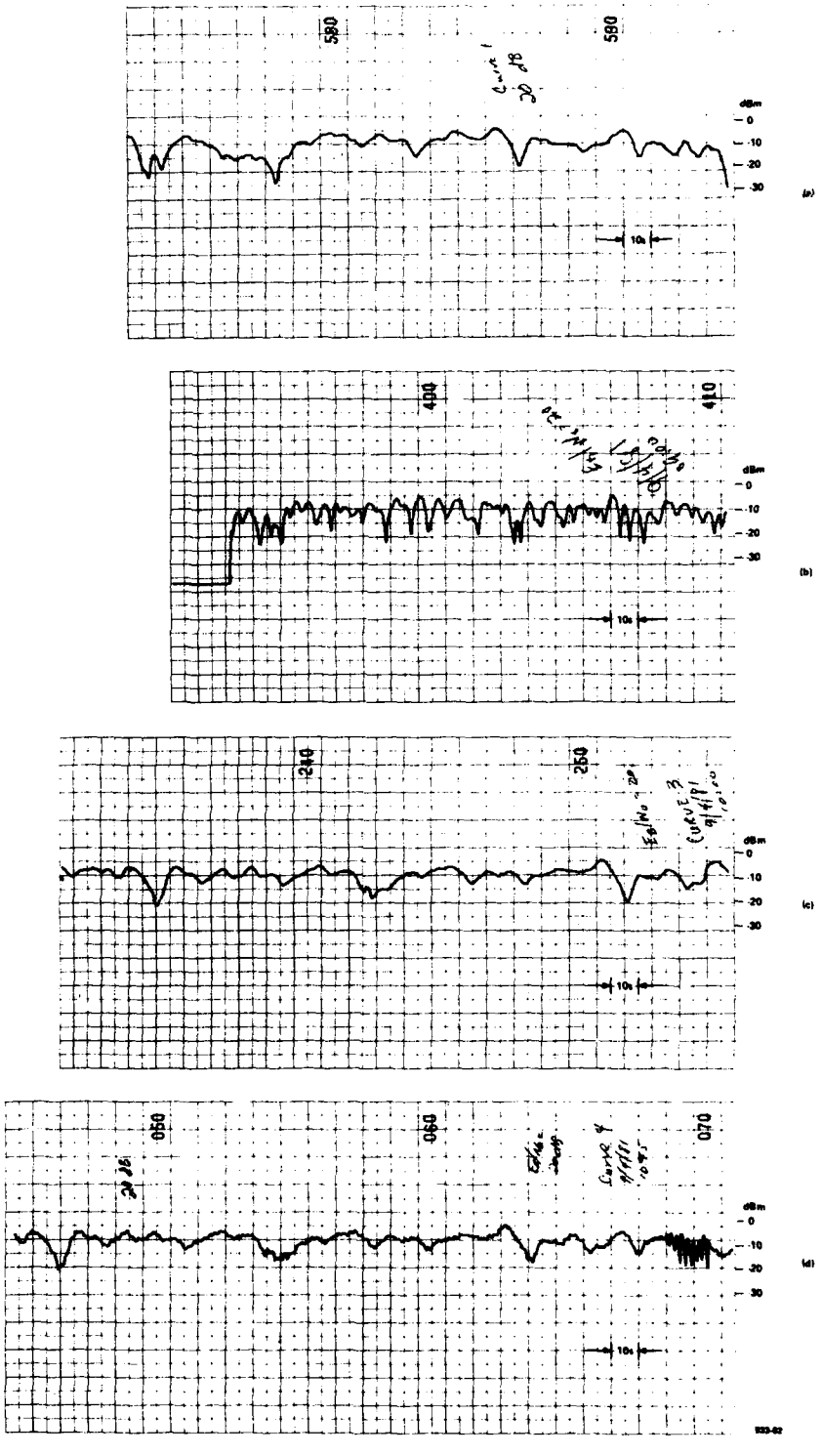


Figure 10-2. Typical AGC Plots: Curve 1 Flat Fading 5 Hz, 25 dB Fading — a, b, c and d

test-record sheet together with the modem settings, one sheet for each of the 34 curves.

The information bit error count (BE) and the information bit count (NB) were read from the display on the IDS test set for all curves except Nos. 17 through 19. Note that these IDS counts are based entirely on information bits actually delivered by the HFWBM to the external data sink, in this case the test set. Specifically, training frames, data frames, rejected by the ARQ threshold test and protocol bits (4 per frame) are excluded in these counts. The total received symbol count (RS) was read from the HFWBM front panel display. This count includes training symbols and repeated symbols. The output information symbol count (NS) was also read from the HFWBM display. This count includes only the information symbols actually delivered to the external data sink. The total ARQ count (NQ) and ARQ retry count (NR) were read from the HFWBM display for all curves except Nos. 17 through 19. The information symbol error count (SE) was read from the HFWBM display for curves 17 through 19 since those tests used the internal error rate test pattern. The observed values of BE (or SE), NB, RS, NS, NQ and NR were all hand-recorded on the reverse side of the individual test record sheets along with the corresponding value of E_b/N_o for each test. The complete set of values constituting the global data base of raw measurements is given in Appendix A. This data base serves as the starting point for further data reduction and analysis.

10.1.4 Data Reduction

The raw measurements from the tests using the DICEF HF media simulator were keyed into an ASCII data file on GTE's DEC-20 computer. The processing applied to the file given in Appendix A included the following:

- Editing and reformatting
- Error rate and throughput computations
- Plotting.

The editing process consisted of stripping off the comments, removal of duplicate or obviously anomalous points, and the addition of some curves representing theoretical data and measured data on other (i.e., multitone) modems for comparison plots (see Section 10.3). The edited data was reformatted into a binary file for further processing.

Bit error rates for each curve were computed using P_b = BE/NB, and throughputs were computed from TPUT = NS/RS. In the case of curves 17 through 19, symbol error rates were computed as P_E = SE/NS.

Computer plot routines were used to set up and plot curves of P_b versus E_b/N_o (or P_E vs. SNR), TPUT versus E_b/N_o, and P_b versus TPUT.

10.2 Performance Results

The two most significant measures which characterize the performance of the HFWBM equipment operating in its ARQ mode are the bit error rate and throughput. These are shown in Figures 10-3 through 10-36 which show the plotted DICEF test results corresponding to curve numbers 1 through 34, respectively. The performance results for one additional curve, not part of the original test procedure, are shown in Figure 10-37. The channel setup for

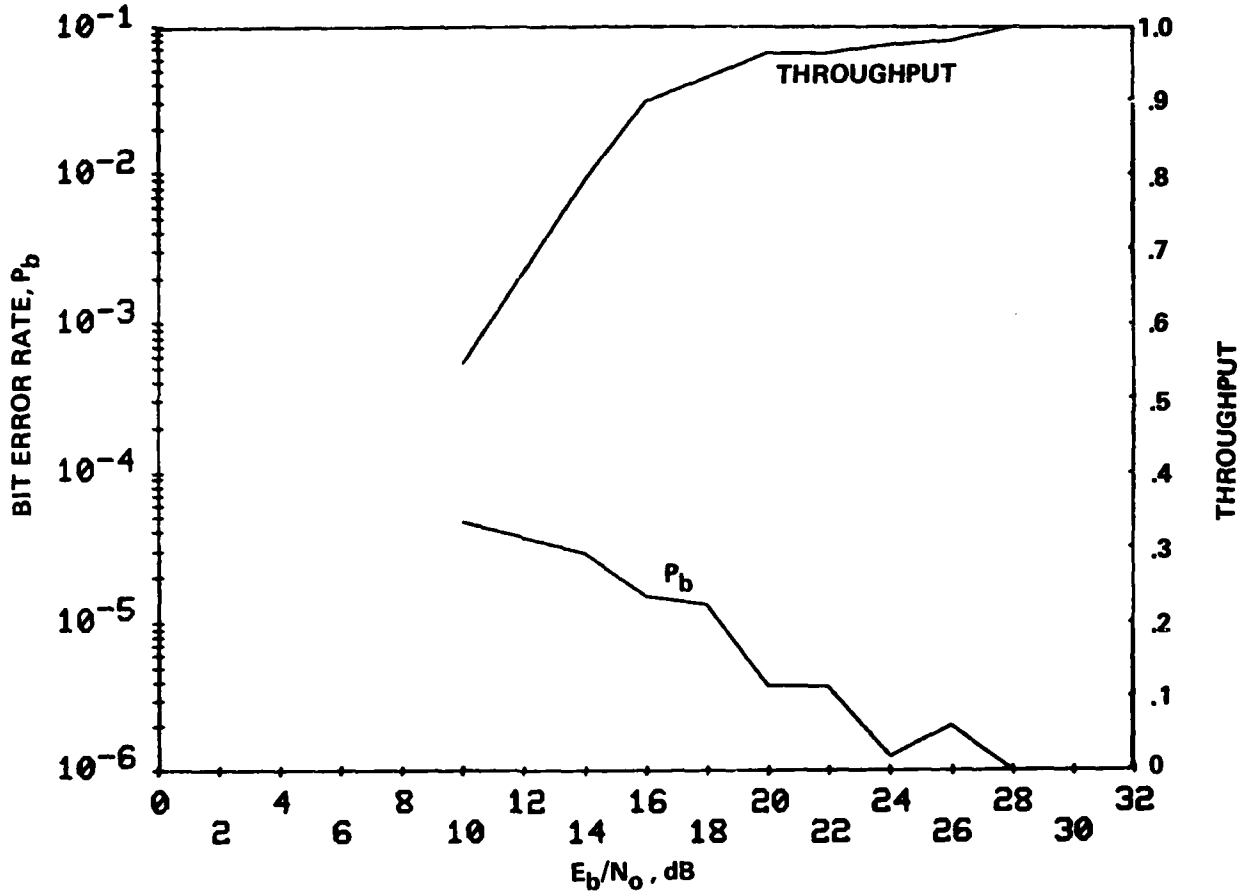


Figure 10-3. Bit Error Rate and Throughput versus Signal-to-Noise Ratio for $n = 1$, $\overline{A}_1 = \infty$, $\tilde{A}_1 =$ 10 dB, $\nu_1 = 0$ Hz, $2\sigma_1 = .05$ Hz, T/2 (8,3) Equalizer, 4800 b/s, 10 dB ARQ Threshold

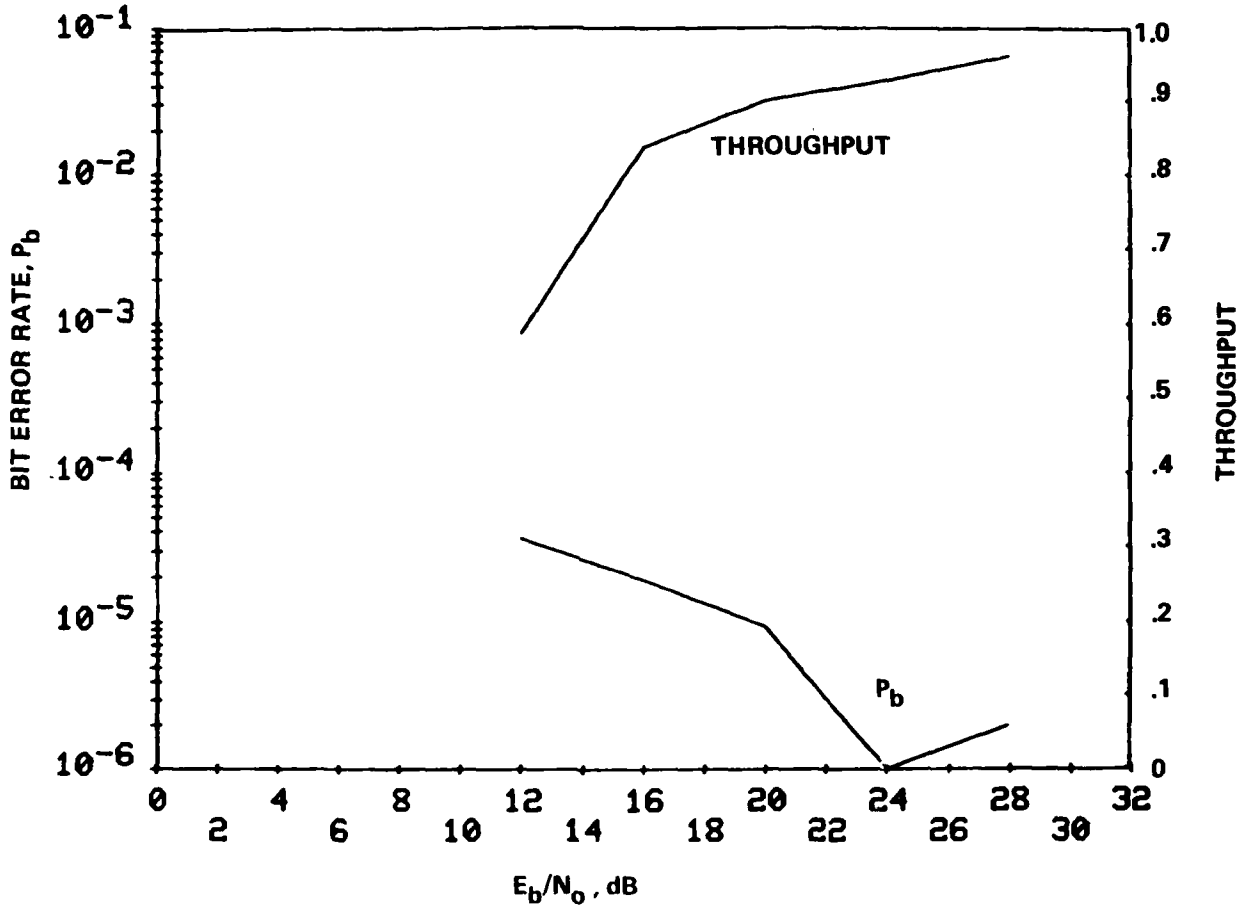


Figure 10-4. Bit Error Rate and Throughput versus Signal-to-Noise Ratio for $n = 1$, $\overline{A}_1 = \infty$, $\hat{A}_1 =$ 10 dB, ν_1 0 Hz, $2\sigma_1$ .1 Hz, T 2 (8.3) Equalizer, 4800 b s, 10 dB ARQ Threshold

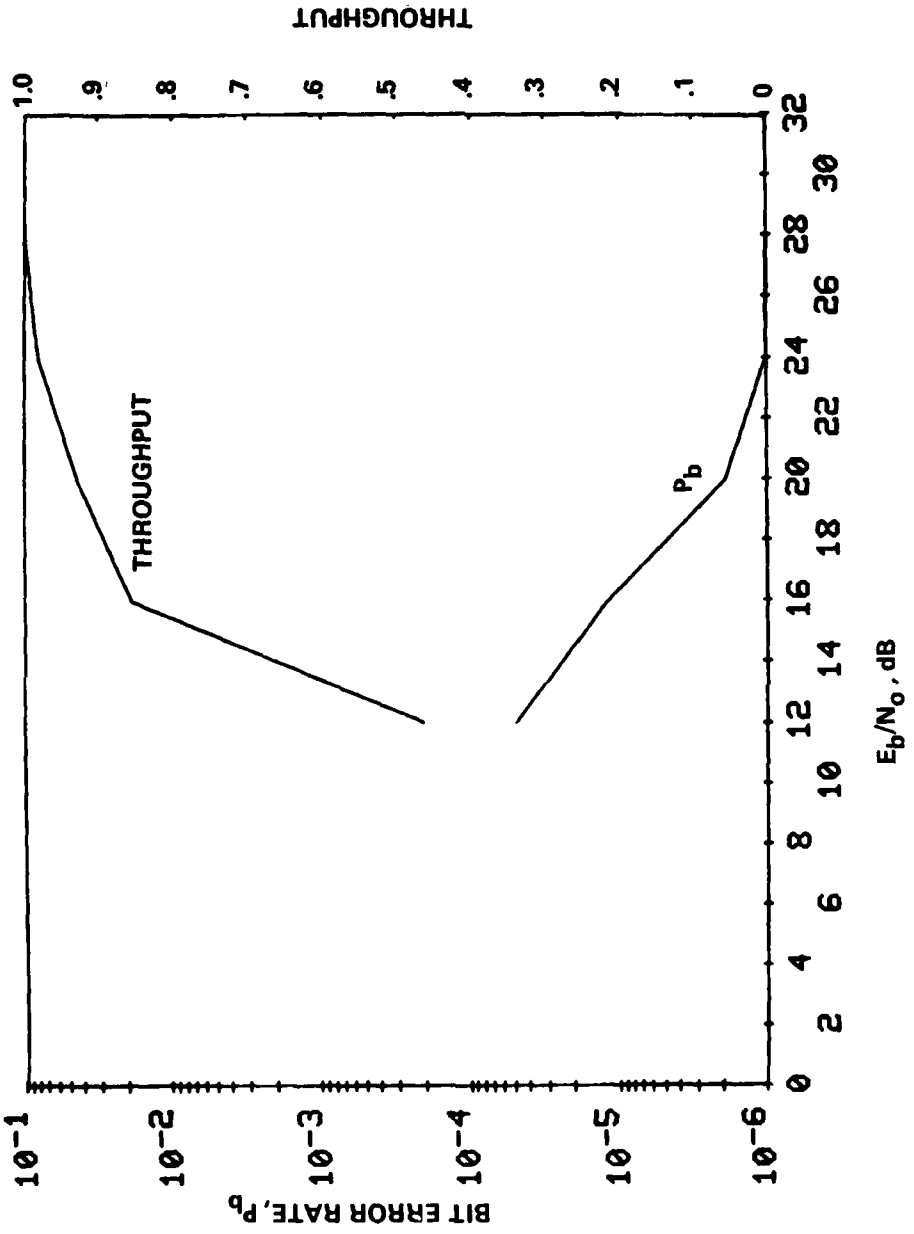


Figure 10-5. Bit Error Rate and Throughput versus Signal-to-Noise Ratio for $n=2$, $\overline{A}_1 = \overline{A}_2 = \infty$, $\hat{A}_1 = \hat{A}_2 = 13$ dB, $\nu_2 = \nu_1 = 0$ Hz, $2\sigma_1 = 2\sigma_2 = .05$ Hz, $\tau_2 - \tau_1 = .4$ ms, T/2 (8,3) Equalizer, 4800 b/s, 10 dB ARQ Threshold

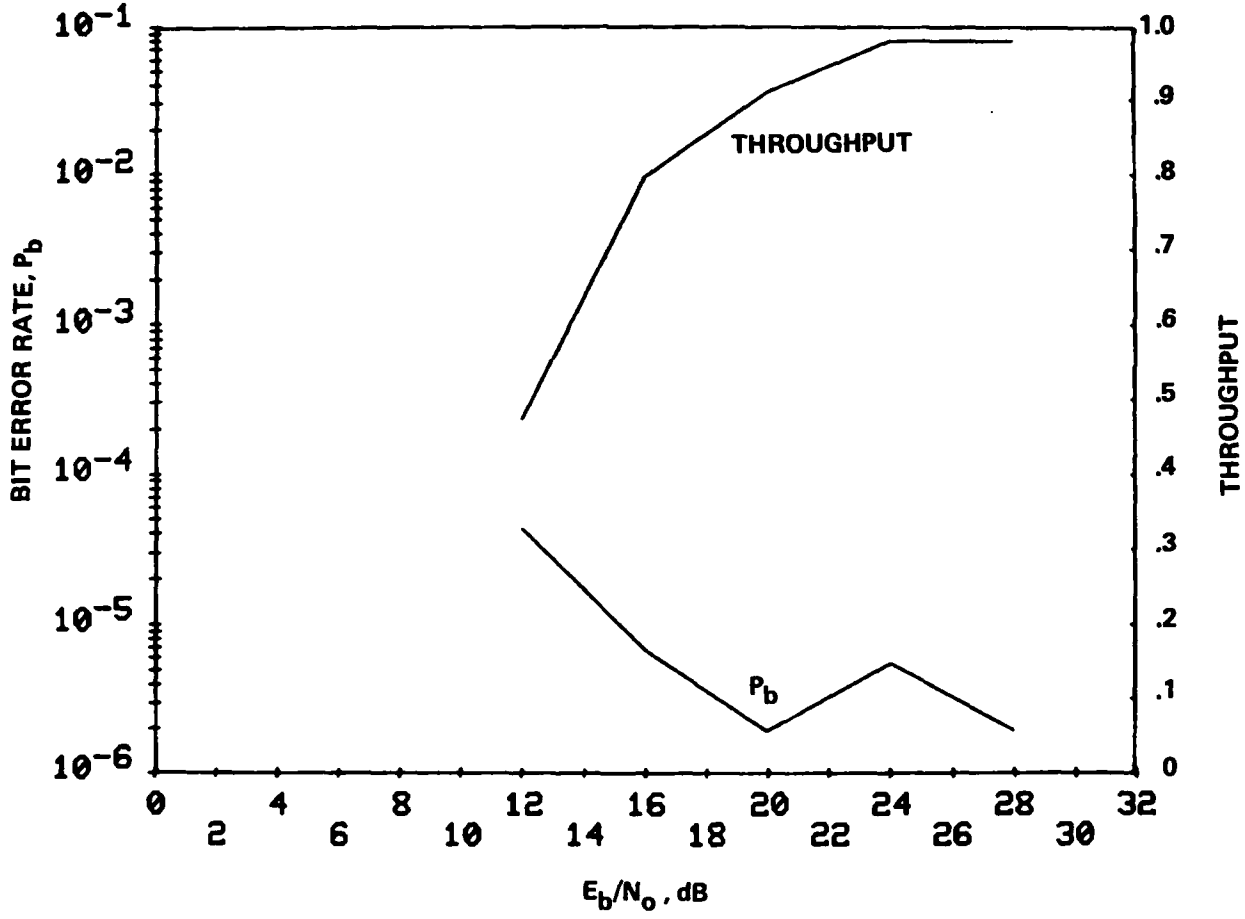


Figure 10-6. Bit Error Rate and Throughput versus Signal-to-Noise Ratio for n = 2, $\overline{A}_1 = \overline{A}_2 = \infty$, $\tilde{A}_1 = \tilde{A}_2 = 13$ dB, $\nu_2 = -\nu_1 = .25$ Hz, $2\sigma_1 = 2\sigma_2 = .05$ Hz, $\tau_2 - \tau_1 = .4$ ms, T/2 (8,3) Equalizer, 4800 b/s, 10 dB ARQ Threshold

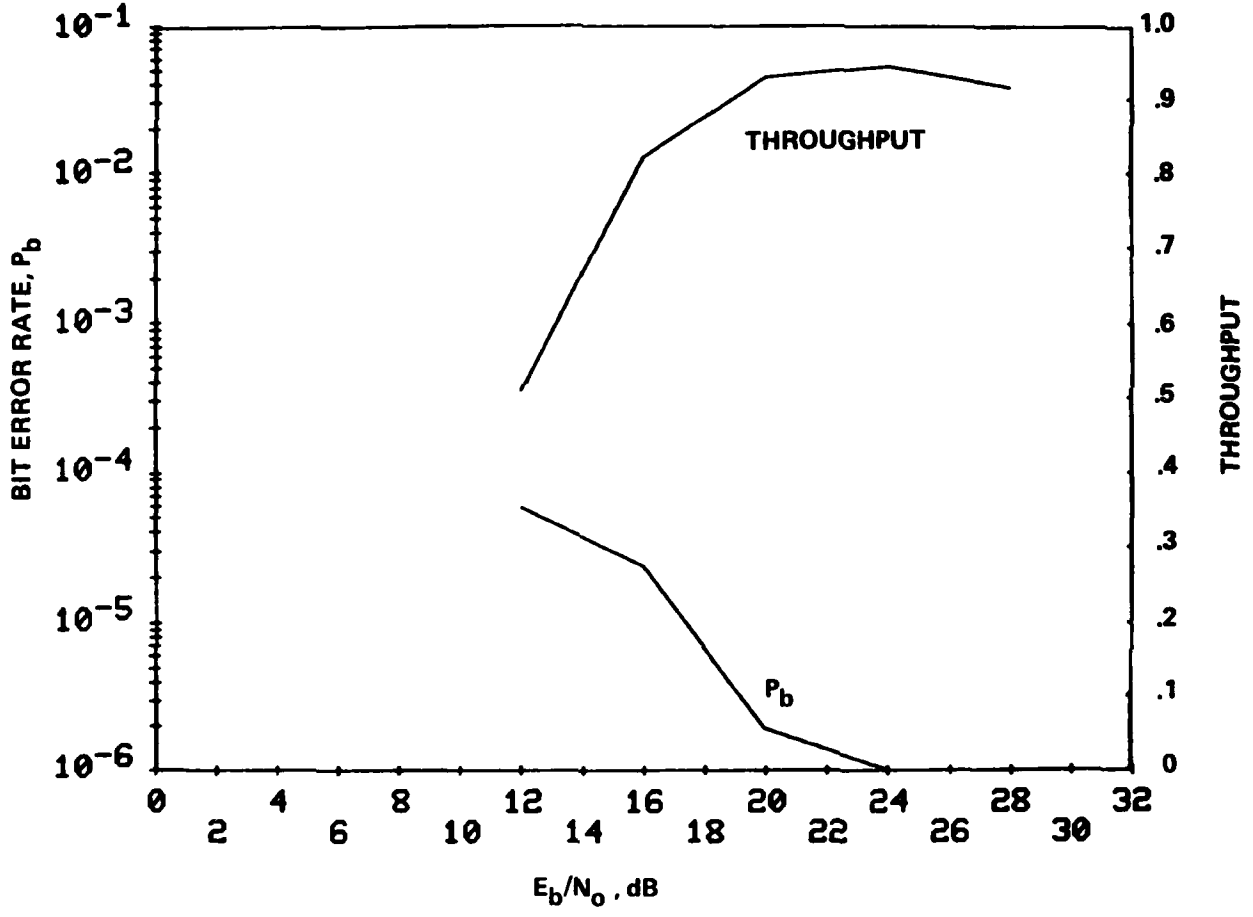


Figure 10-7. Bit Error Rate and Throughput versus Signal-to-Noise Ratio for n = 2, $\overline{A}_1 = \overline{A}_2 = x$, $A_1 = A_2 = 13$ dB, $\nu_2 = \nu_1 = .5$ Hz, $2\nu_1 = 2\nu_2 = .05$ Hz, $\tau_2 - \tau_1 = .4$ ms, T/2 (8,3) Equalizer, 4800 b/s, 10 dB ARQ Threshold

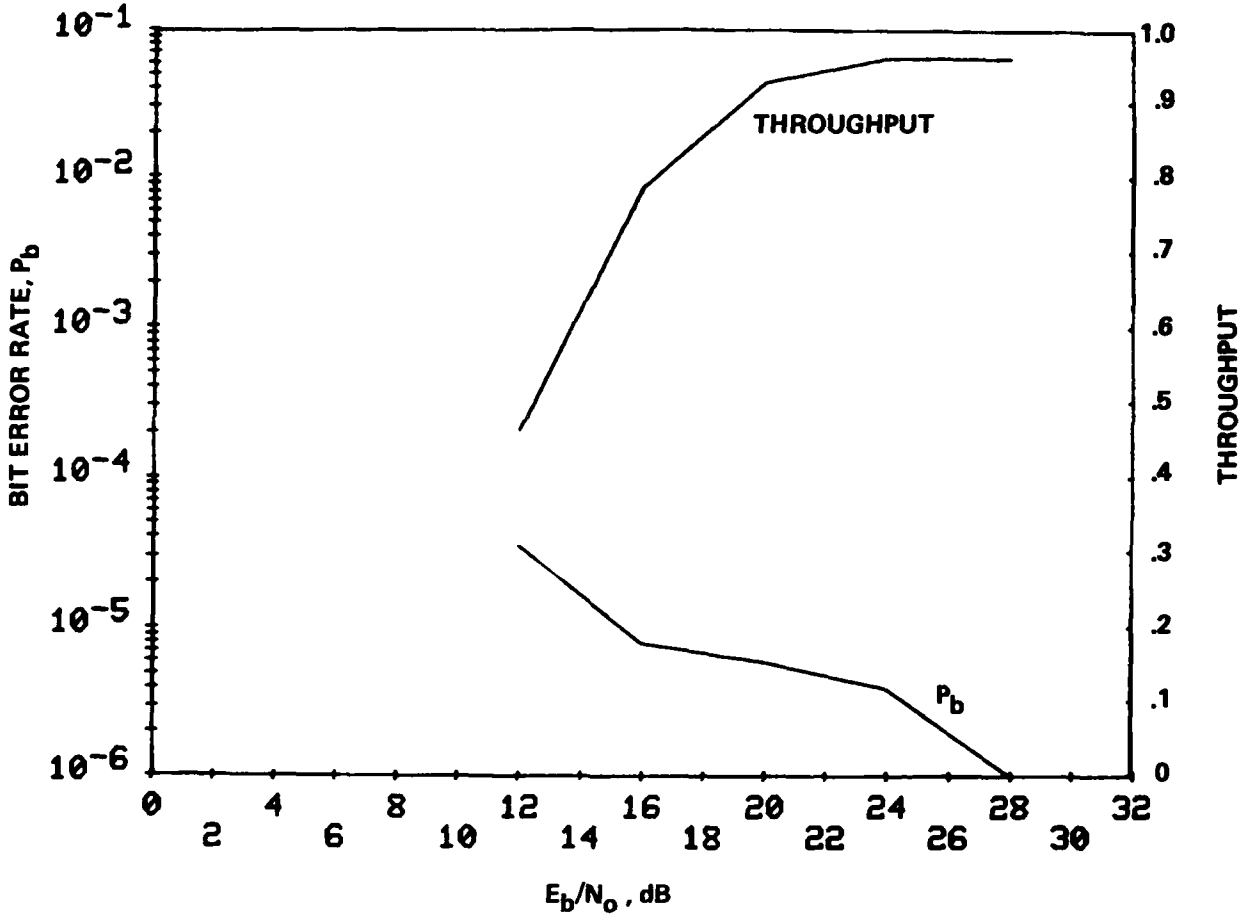


Figure 10-8. Bit Error Rate and Throughput versus Signal-to-Noise Ratio for $n=2$, $\bar{A}_1 = \bar{A}_2 = \infty$, $\tilde{A}_1 = \tilde{A}_2 = 13$ dB, $\nu_2 = -\nu_1 = .5$ Hz, $2\sigma_1 = 2\sigma_2 = .05$ Hz, $\tau_2 - \tau_1 = .4$ ms, T (4,3) Equalizer, 4800 b/s, 10 dB ARQ Threshold

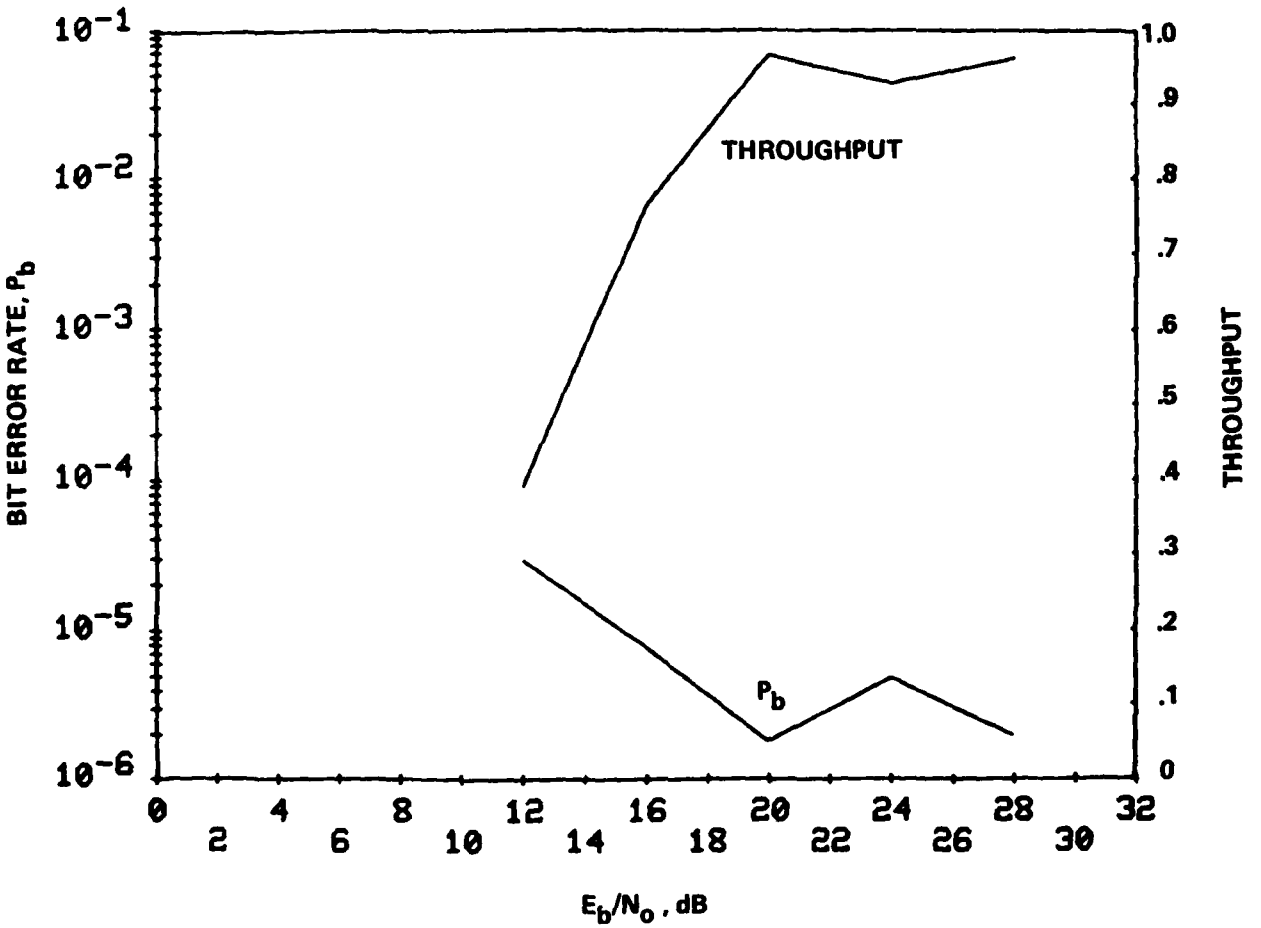


Figure 10-9. Bit Error Rate and Throughput versus Signal-to-Noise Ratio for $n=2$, $\overline{A}_1 = \overline{A}_2 = \infty$, $\tilde{A}_1 = \tilde{A}_2 = 13$ dB, $\nu_2 = -\nu_1 = 1$. Hz, $2\sigma_1 = 2\sigma_2 = .05$ Hz, $\tau_2 - \tau_1 = .4$ ms, T/2 (8,3) Equalizer, 4800 b/s, 10 dB ARQ Threshold

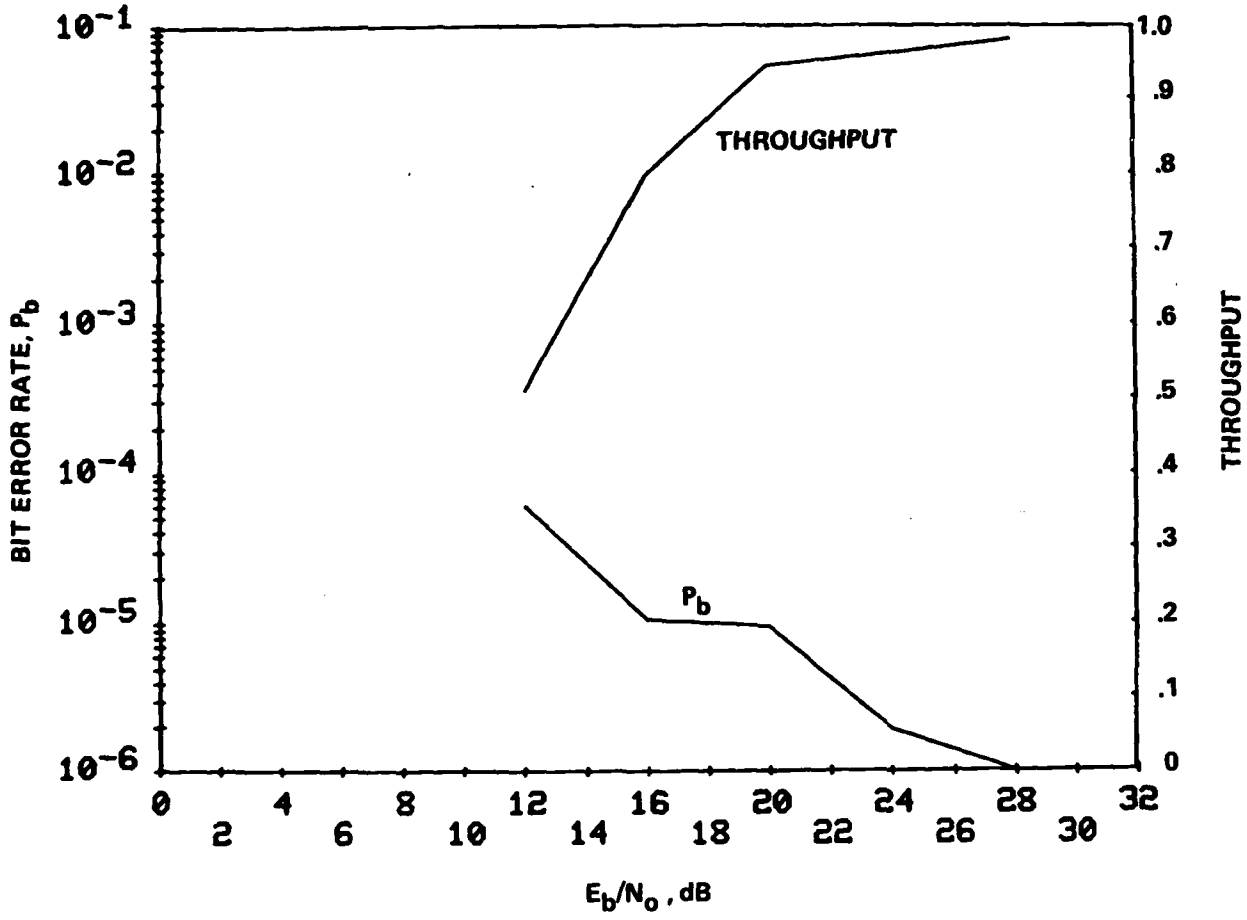


Figure 10-10. Bit Error Rate and Throughput versus Signal-to-Noise Ratio for n = 2, $\overline{A}_1 = \overline{A}_2 \infty$, $\tilde{A}_1 = \tilde{A}_2 = 13$ dB, $\nu_2 = \nu_1 = 0$ Hz, $2\sigma_1 = 2\sigma_2 = .1$ Hz, $\tau_2 - \tau_1 = .4$ ms, T/2 (8,3) Equalizer, 4800 b/s, 10 dB ARQ Threshold

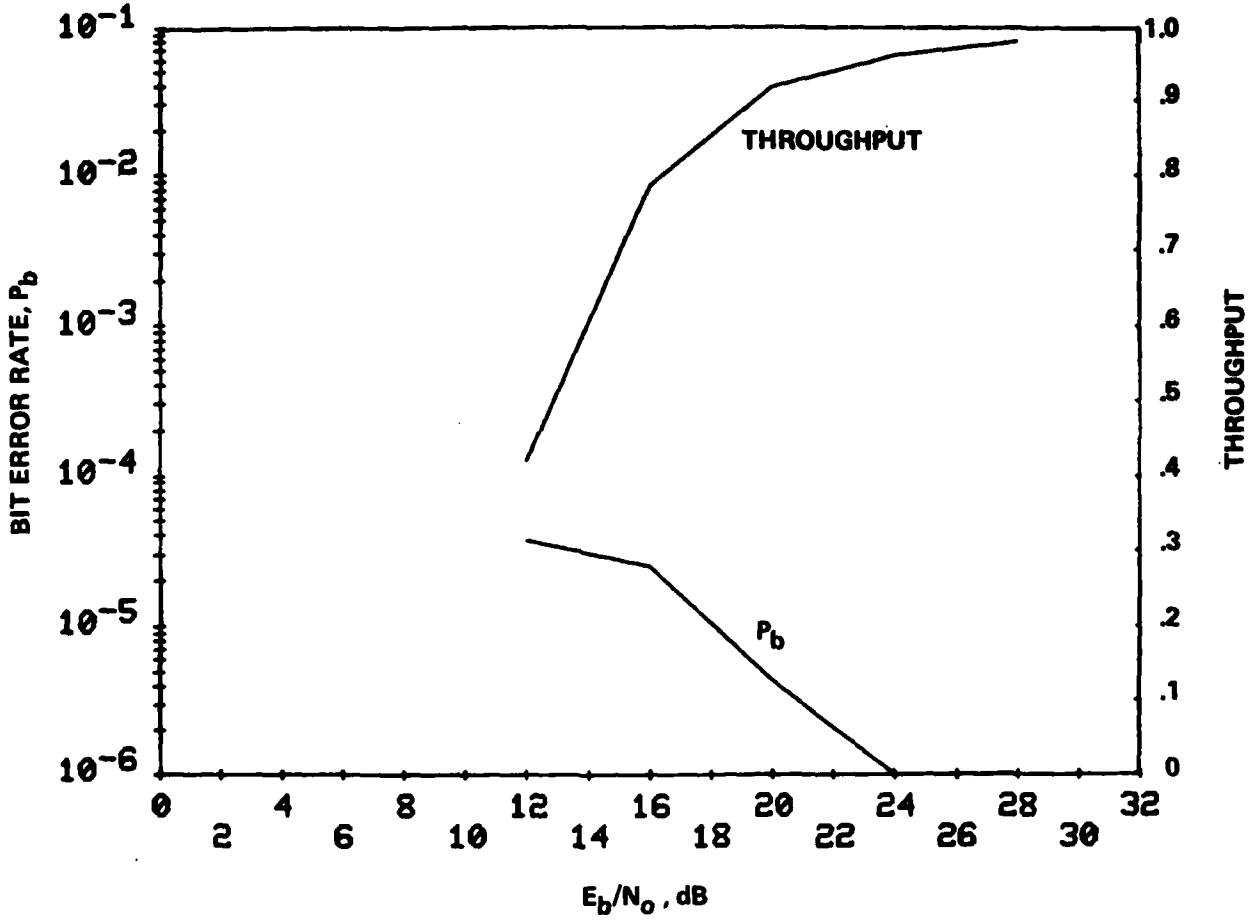


Figure 10-11. Bit Error Rate and Throughput versus Signal-to-Noise Ratio for n = 2, $\overline{A}_1 = \overline{A}_2 = \infty$, $\tilde{A}_1 = \tilde{A}_2 = 13$ dB, $\nu_2 = -\nu_1 = .5$ Hz, $2\sigma_1 = 2\sigma_2 = .1$ Hz, $\tau_2 - \tau_1 = .4$ ms, T/2 (8,3) Equalizer, 4800 b/s, 10 dB ARQ Threshold

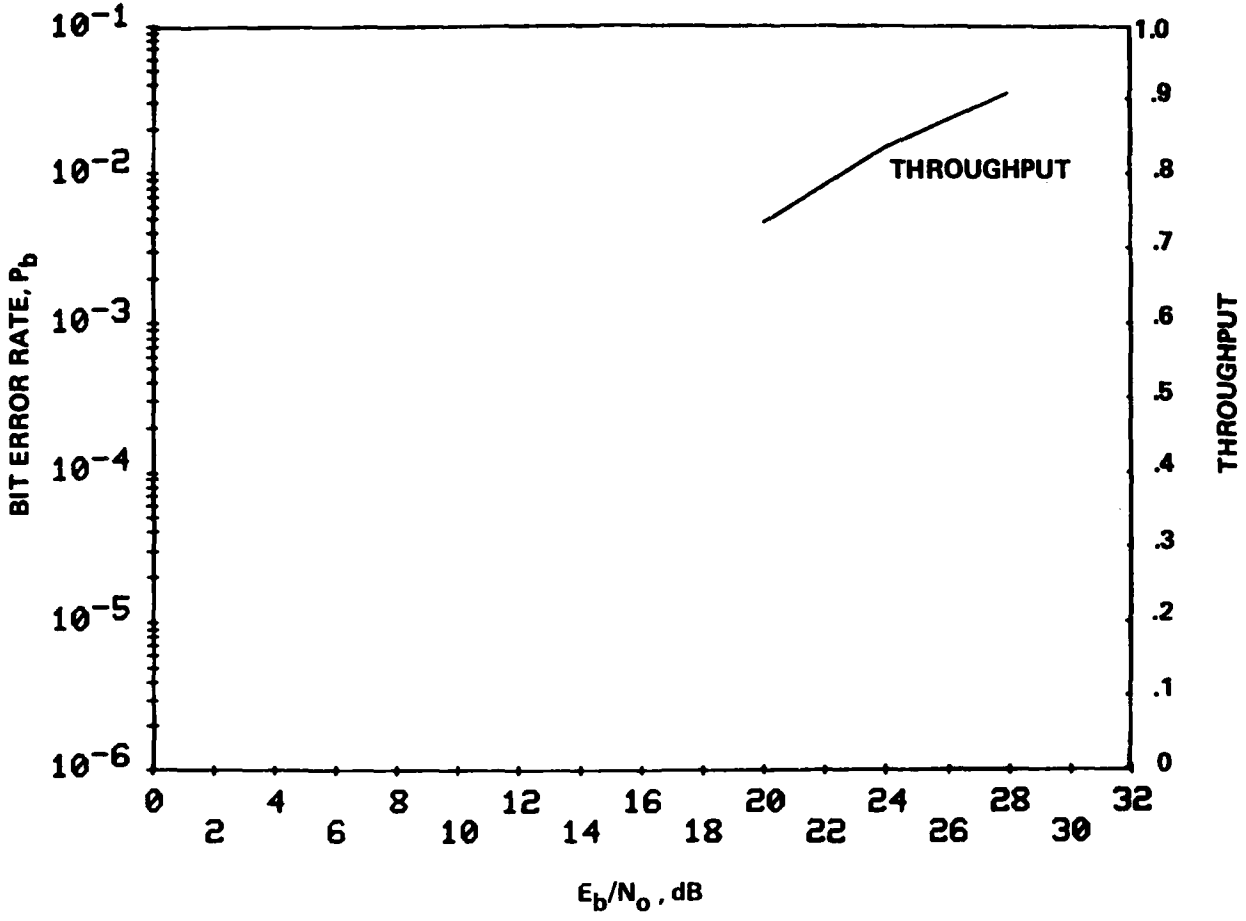


Figure 10-12. Bit Error Rate and Throughput versus Signal-to-Noise Ratio for n = 2, $\bar{A}_1 = \bar{A}_2 = \infty$, $\tilde{A}_1$ = 26 dB, $\tilde{A}_2$ = 10 dB, $\nu_2 = \nu_1$ = .5 Hz, $2\sigma_1 = 2\sigma_2$ = .05 Hz, $\tau_2 - \tau_1$ = 1.2 ms, T/2 (14,6) Equalizer, 2400 b/s, 10 dB ARQ Threshold

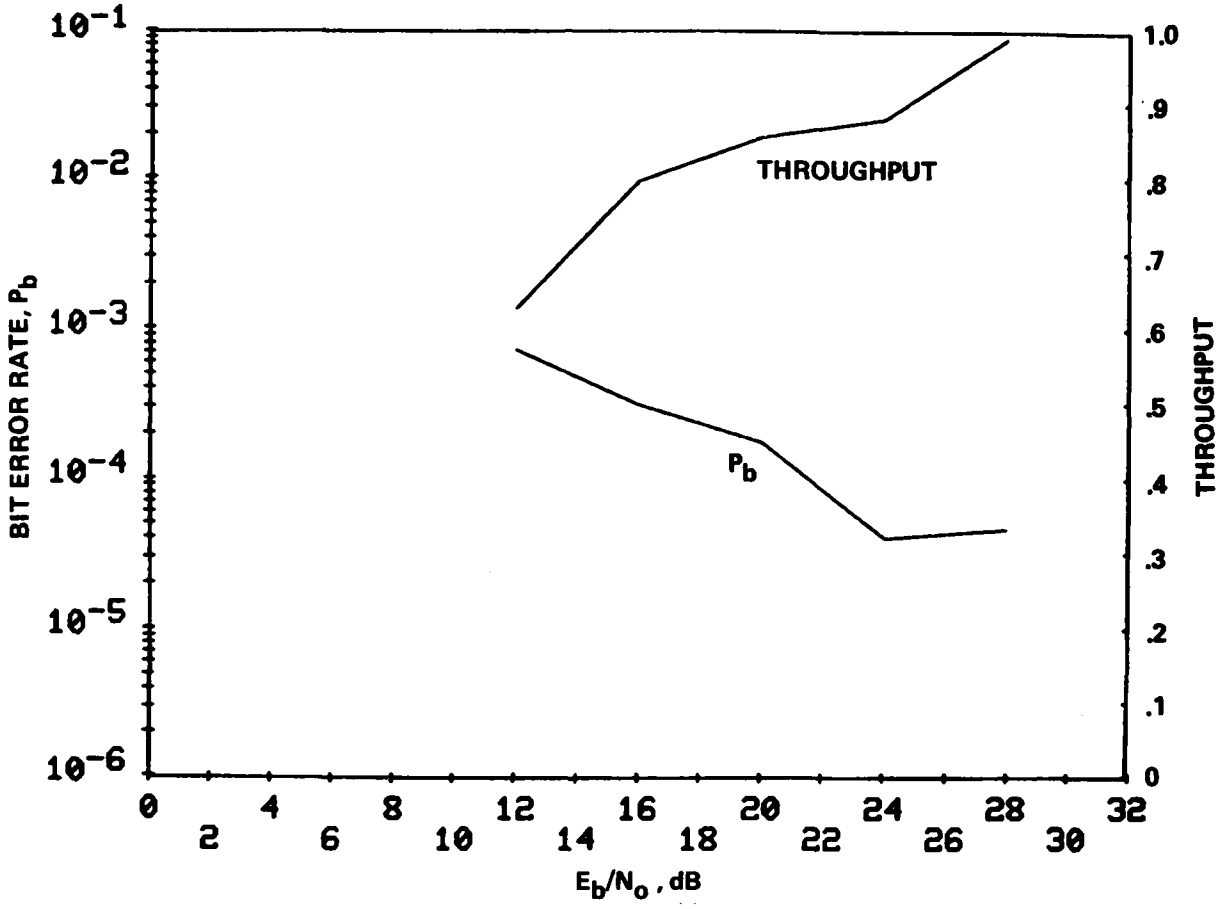


Figure 10-13. Bit Error Rate and Throughput versus Signal-to-Noise Ratio for n = 2, $\overline{A}_1 = \overline{A}_2 = \infty$, $\bar{A}_1$ = 26 dB, $\bar{A}_2$ = 10 dB, $\nu_2 = -\nu_1$ = .5 Hz, $2\sigma_1 = 2\sigma_2$ = .05 Hz, $\tau_2 - \tau_1$ = 1.2 ms, T/2 (14,6) Equalizer, 4800 b/s, 8 dB ARQ Threshold

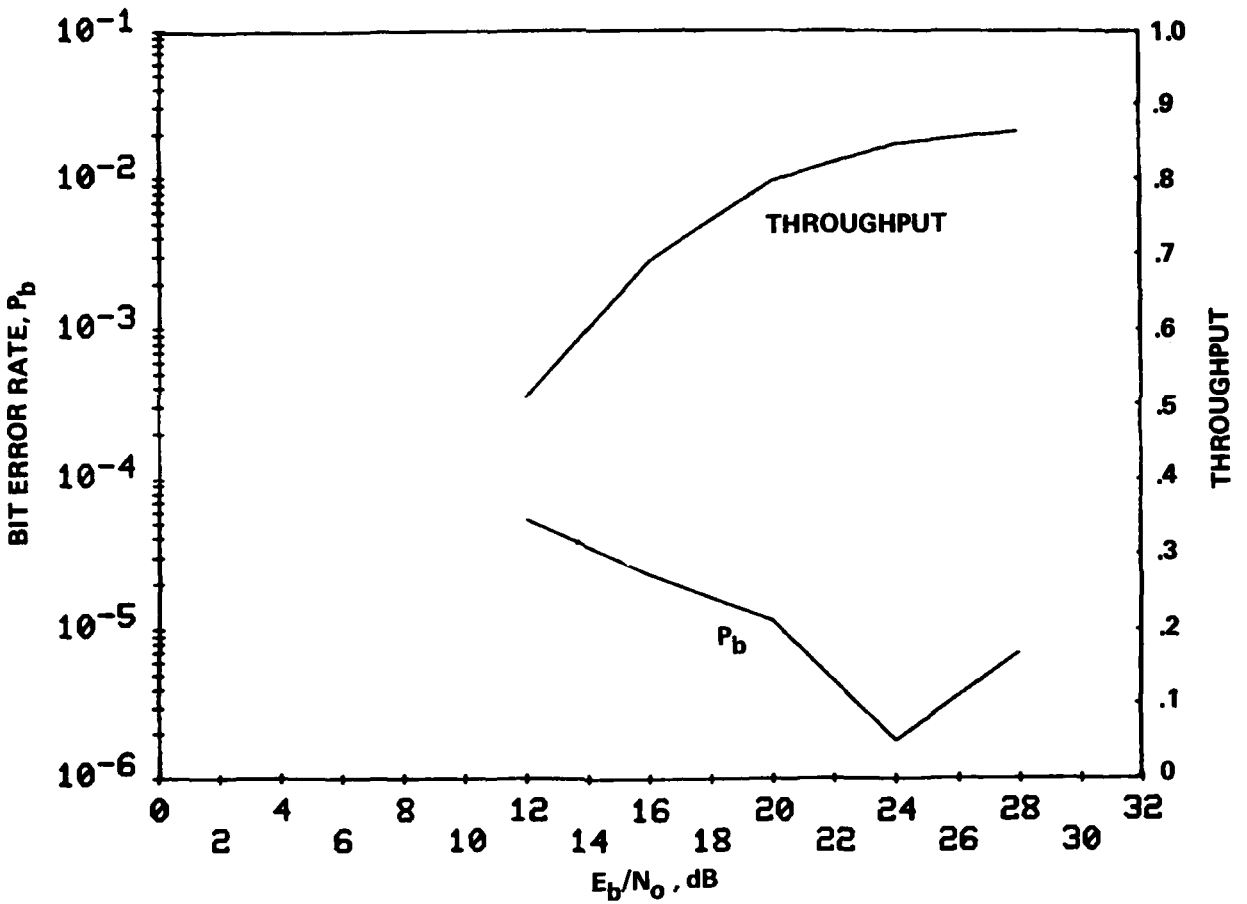


Figure 10-14. Bit Error Rate and Throughput versus Signal-to-Noise Ratio for n = 2, $\overline{A}_1 = \overline{A}_2 = \infty$, $\tilde{A}_1$ = 26 dB, $\tilde{A}_2$ = 10 dB, $\nu 2 \approx -\nu_1$ = .5 Hz, $2\sigma_1 = 2\sigma_2$ = .05 Hz, $\tau_2 - \tau_1$ = 1.2 ms, T/2 (14,6) Equalizer, 4800 b/s, 10 dB ARQ Threshold

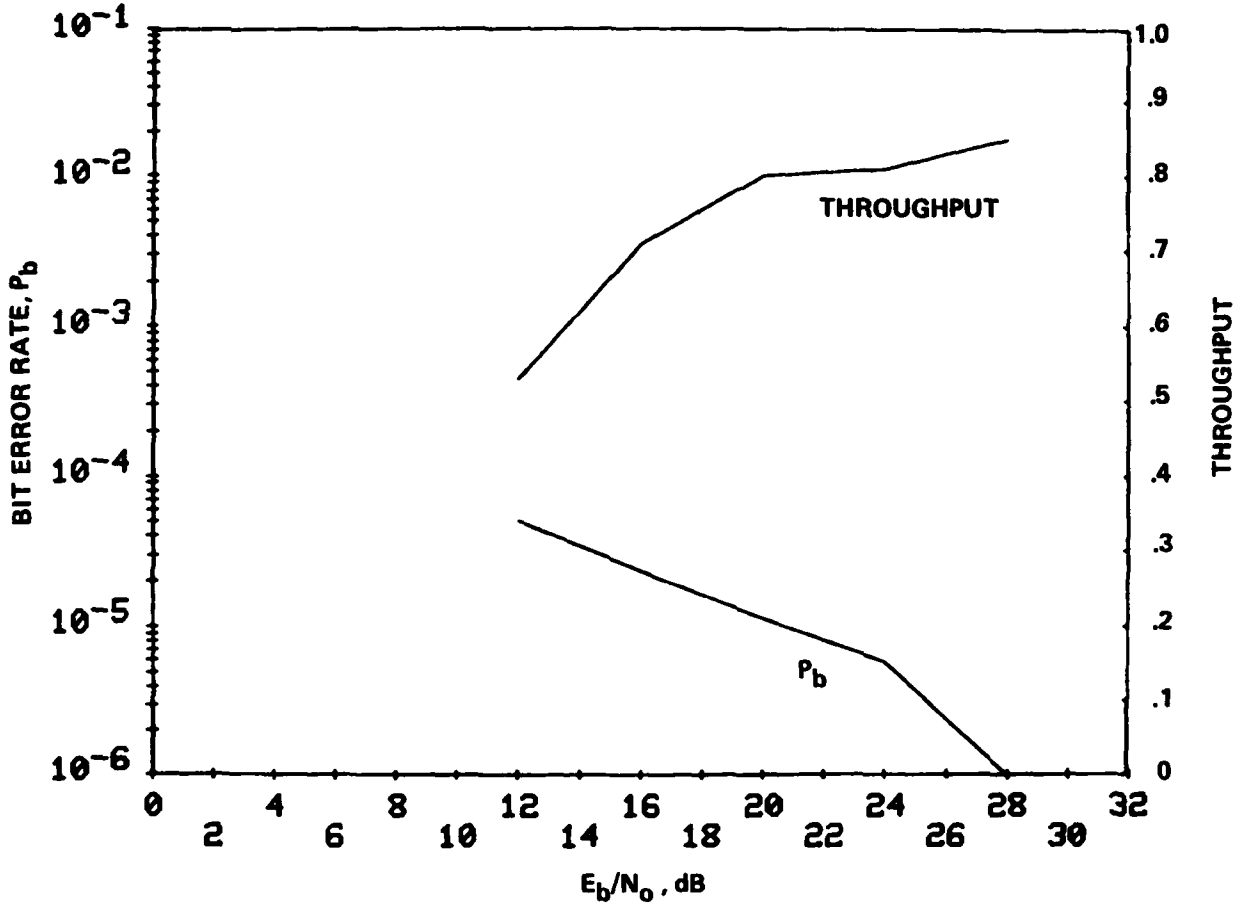


Figure 10-15. Bit Error Rate and Throughput versus Signal-to-Noise Ratio for n = 2, $\overline{A}_1 = \overline{A}_2 = \infty$, $\tilde{A}_1$ = 26 dB, $\tilde{A}_2$ = 10 dB, $\nu_2 = -\nu_1$ = .5 Hz, $2\sigma_1 = 2\sigma_2$ = .05 Hz, $\tau_2 - \tau_1$ = 1.2 ms, T (7,6) Equalizer, 4800 b/s, 10 dB ARQ Threshold

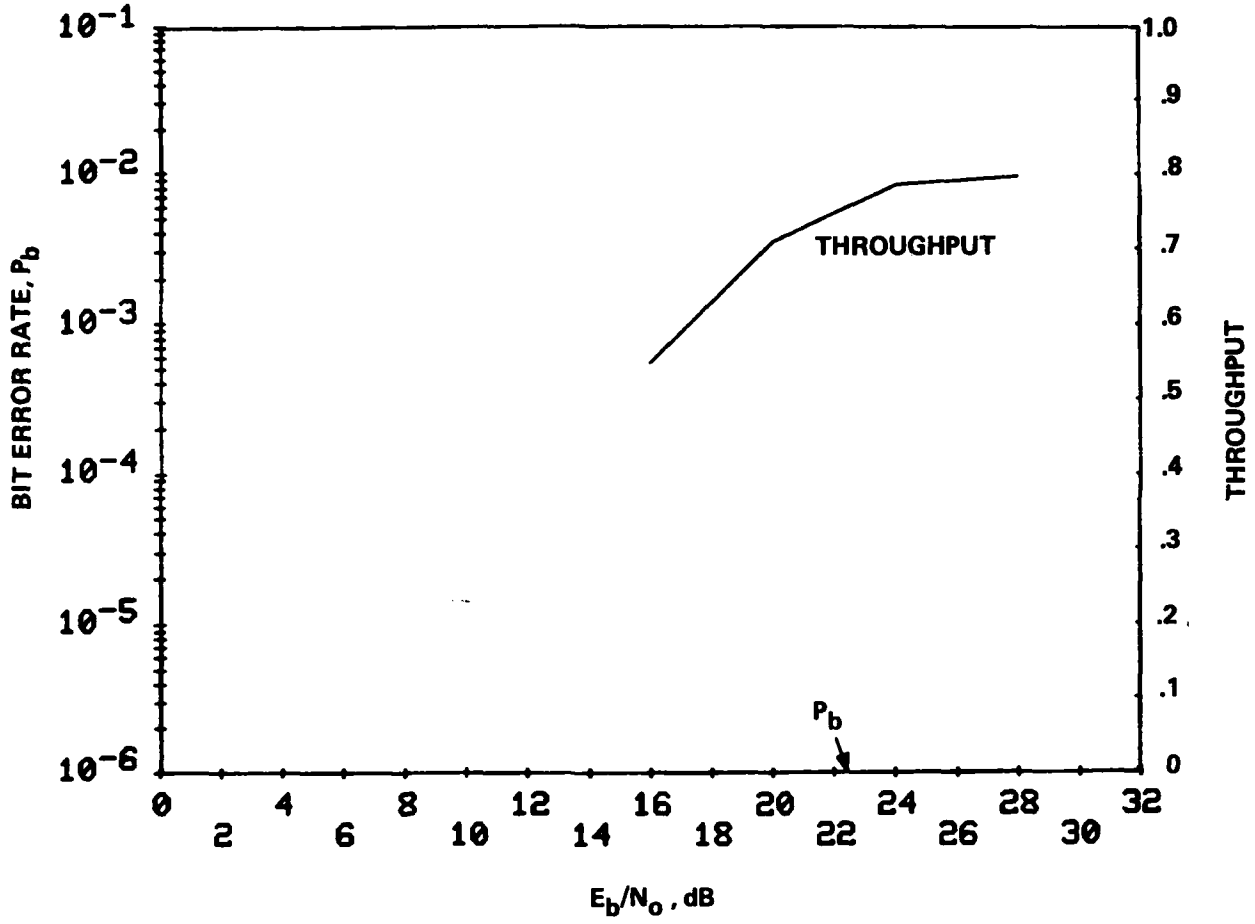


Figure 10-16. Bit Error Rate and Throughput versus Signal-to-Noise Ratio for n = 2, $\overline{A}_1 = \overline{A}_2 = \infty$, $\tilde{A}_1$ = 26 dB, $\tilde{A}_2$ = 10 dB, $\nu_2 = -\nu_1$ = .5 Hz, $2\sigma_1 = 2\sigma_2$ = .05 Hz, $\tau_2 - \tau_1$ = 1.2 ms, T/2 (14,6) Equalizer, 4800 b/s 12 dB ARQ Threshold

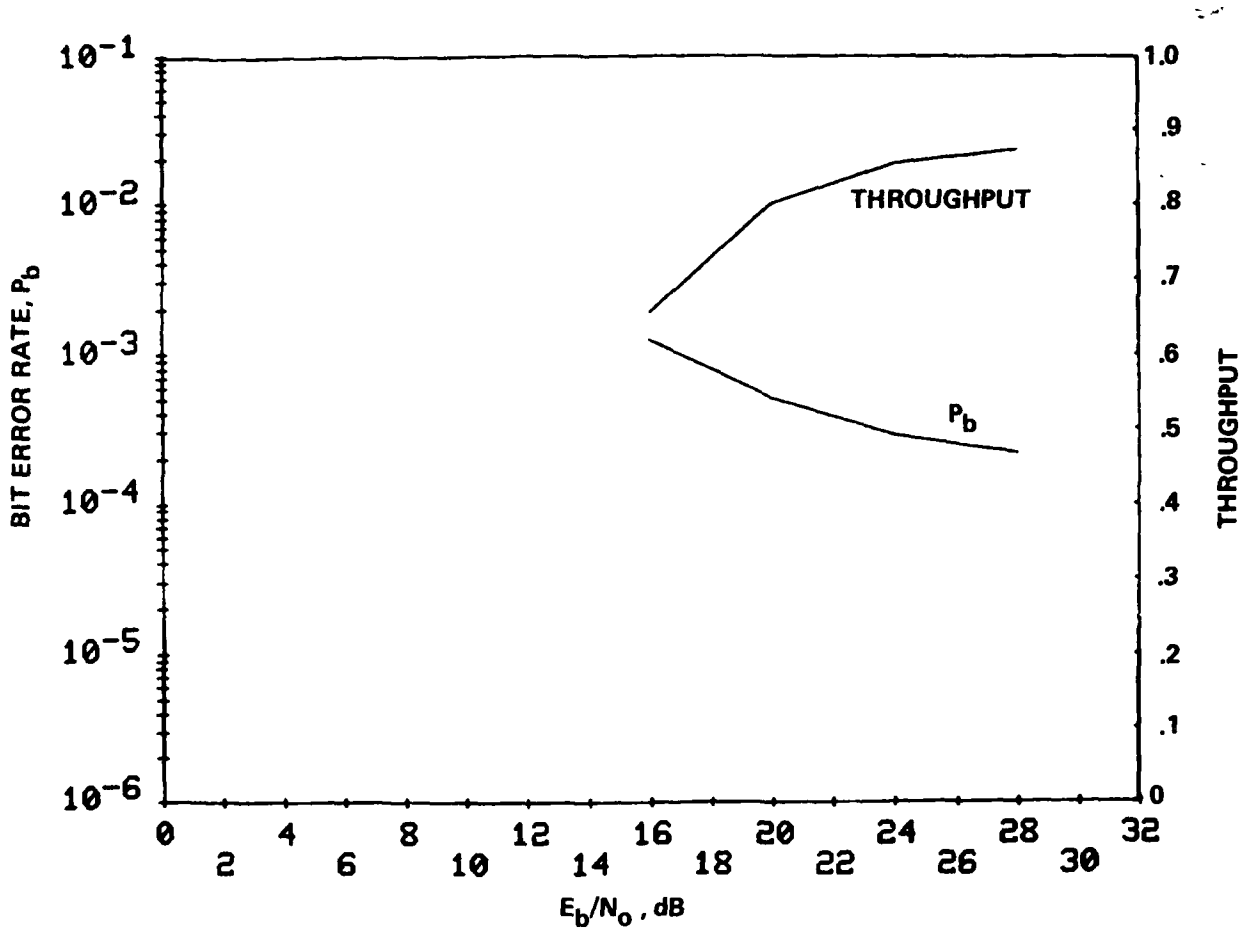


Figure 10-17. Bit Error Rate and Throughput versus Signal-to-Noise Ratio for n = 2, $\overline{A}_1 = \overline{A}_2 = \infty$, $\bar{A}_1 = 26$ dB, $\bar{A}_2 = 10$ dB, $\nu_2 = -\nu_1 = .5$ Hz, $2\sigma_1 = 2\nu_2 = .05$ Hz, $\tau_2 - \tau_1 = 1.2$ ms, T/2 (14,6) Equalizer, 7200 b/s, 12 dB ARQ Threshold

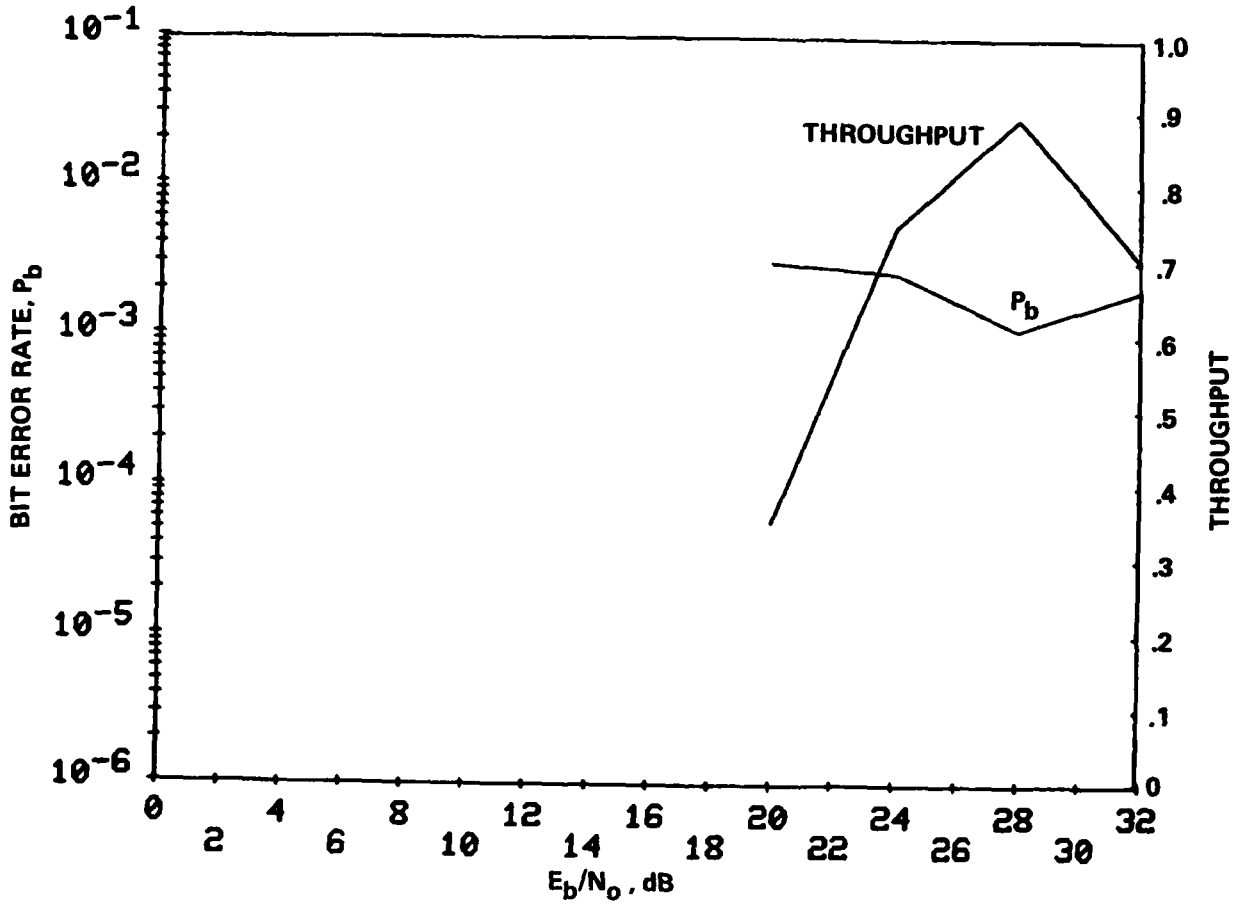


Figure 10-18. Bit Error Rate and Throughput versus Signal-to-Noise Ratio for $n=2$, $\overline{A}_1 = \overline{A}_2 = \infty$, $\tilde{A}_1 = 26$ dB, $\tilde{A}_2 = 10$ dB, $\nu_2 = -\nu_1 = .5$ Hz, $2\sigma_1 = 2\sigma_2 = .05$ Hz, $\tau_2 - \tau_1 = 1.2$ ms, T/2 (14,6) Equalizer, 9600 b/s, 14 dB ARQ Threshold

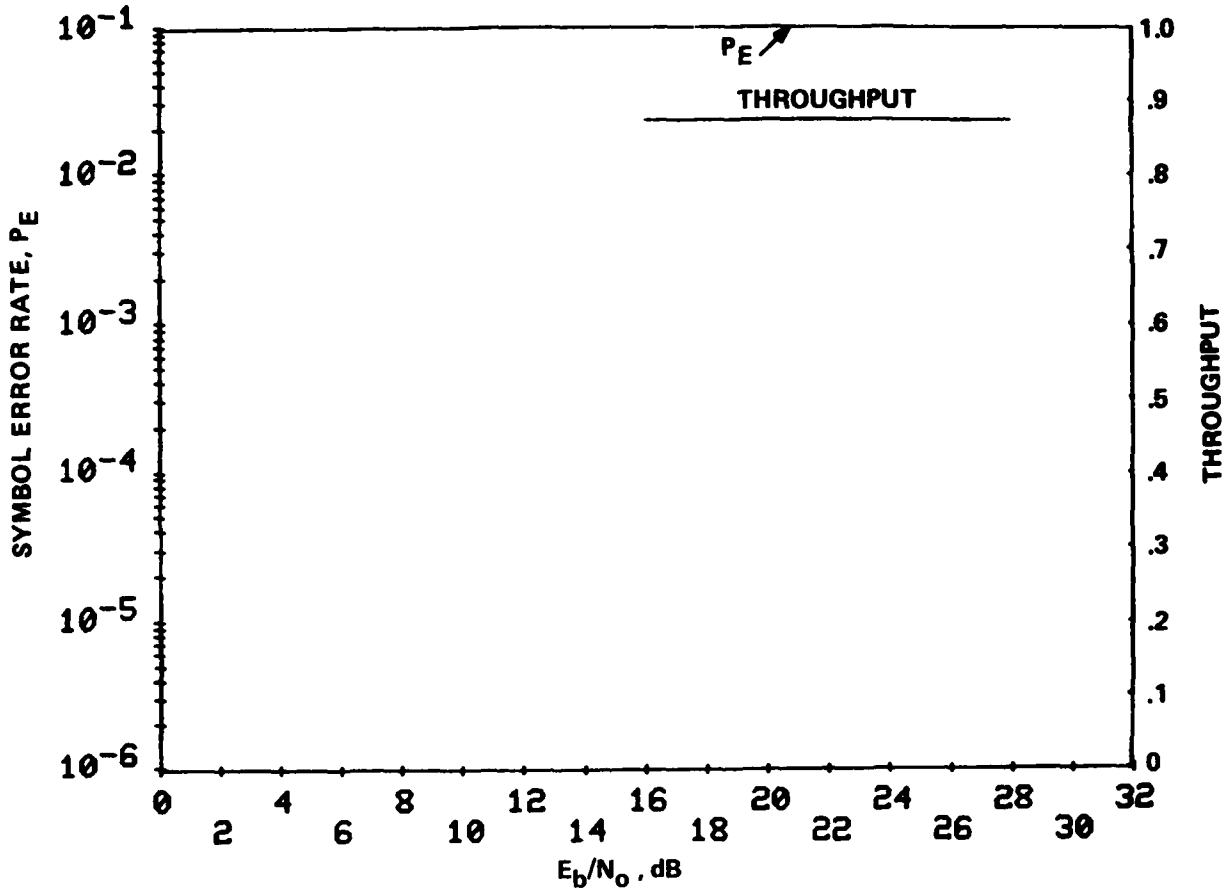


Figure 10-19. Bit Error Rate and Throughput versus Signal-to-Noise Ratio for n = 2, $\bar{A}_1 = \bar{A}_2 = \infty$, $\bar{A}_1 = 26$ dB, $\bar{A}_2 = 10$ dB, $\sigma_2 = \sigma_1 = .5$ Hz, $2\sigma_1 = \sigma_2 = .05$ Hz, $\tau_2 - \tau_1 = 1.2$ ms, T/2 (14,6) Equalizer, 4800 b/s, 12.5% Training

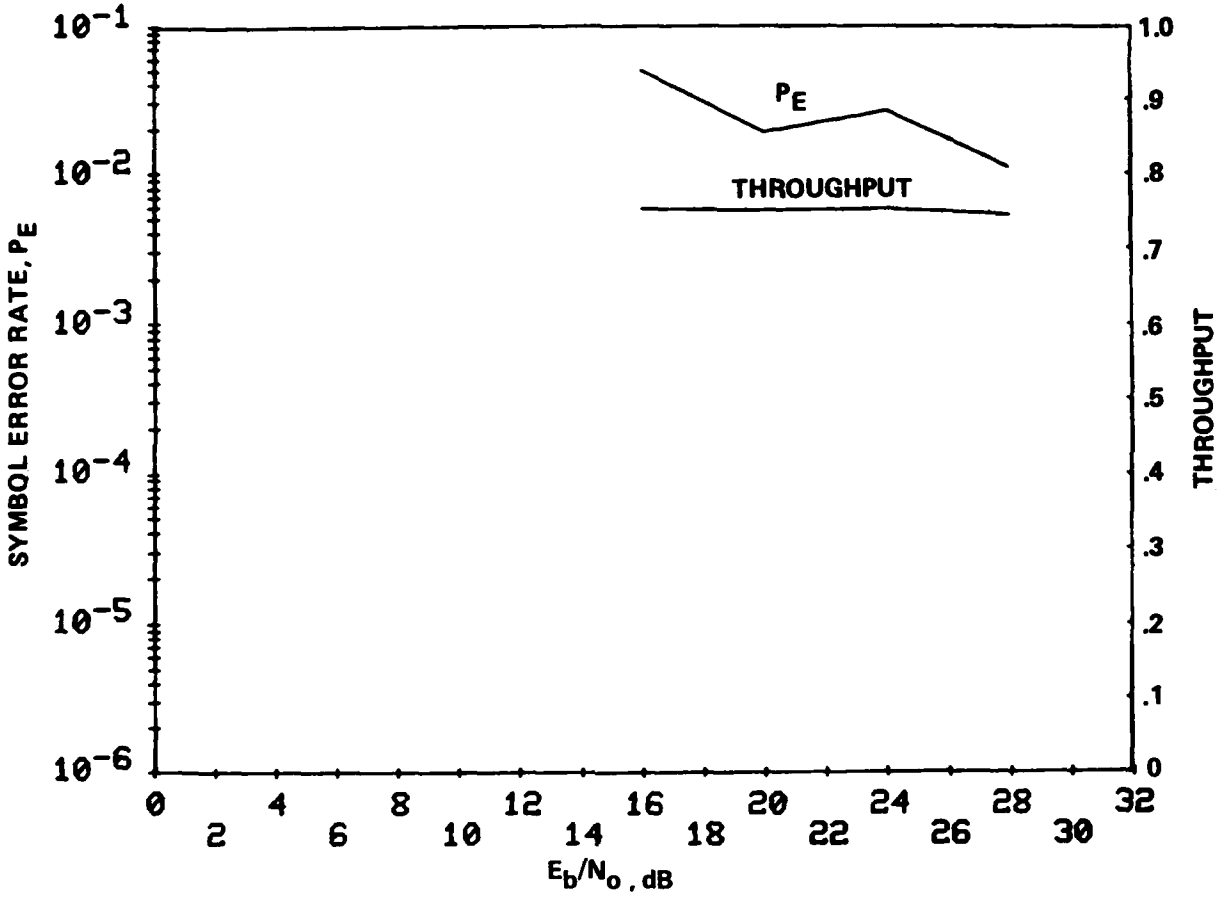


Figure 10-20. Bit Error Rate and Throughput versus Signal-to-Noise Ratio for n = 2, $\bar{A}_1 = \bar{A}_2 = \infty$, $\tilde{A}_1$ = 26 dB, $\tilde{A}_2$ = 10 dB, $\nu_2 = -\nu_1$ = .5 Hz, $2\sigma_1 = 2\sigma_2$ = .05 Hz, $\tau_2 - \tau_1$ = 1.2 ms, T/2 (14,6) Equalizer, 4800 b/s, 25% Training

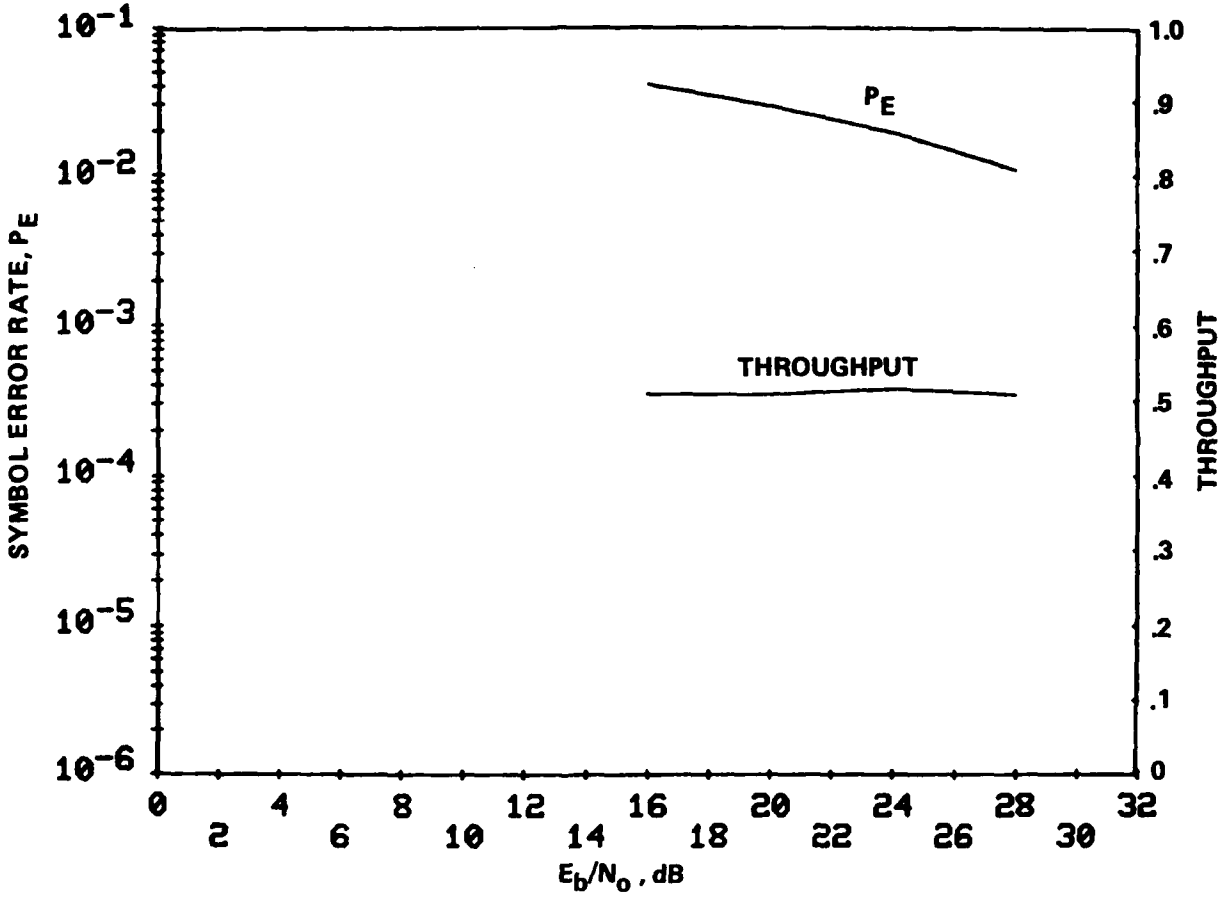


Figure 10-21. Bit Error Rate and Throughput versus Signal-to-Noise Ratio for n = 2, $\overline{A}_1 = \overline{A}_2 = \infty$, $\tilde{A}_1$ = 26 dB, $\tilde{A}_2$ = 10 db, $\nu_2 = -\nu_1$ = .5 Hz, $2\sigma_1 = 2\sigma_2$ = .05 Hz, $\tau_1 - \tau_2$ = 1.2 ms, T/2 (14,6) Equalizer, 4800 b/s, 50% Training

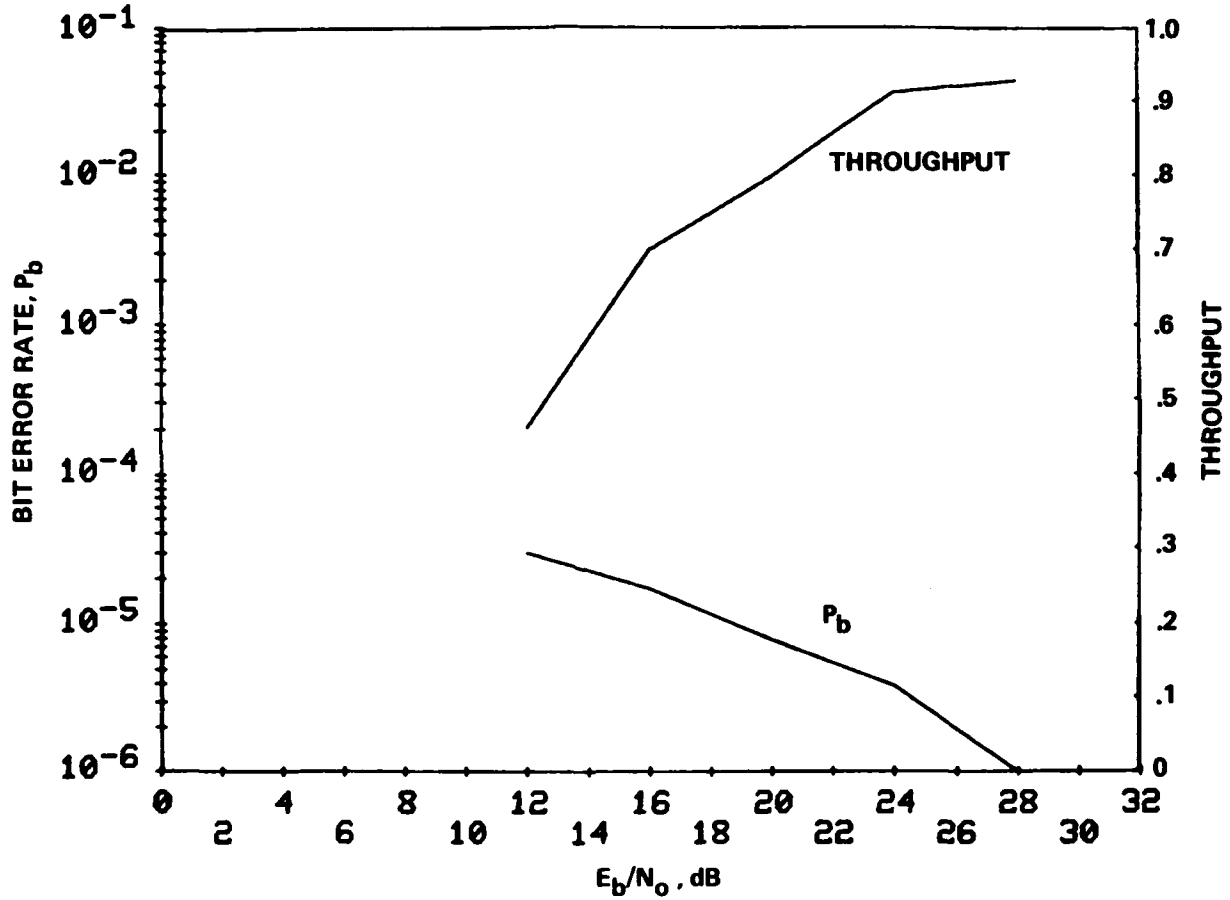


Figure 10-22. Bit Error Rate and Throughput versus Signal-to-Noise Ratio for n = 2, $\overline{A}_1 = \overline{A}_2 = \infty$, $\hat{A}_1$ = 26 dB, $\hat{A}_2$ = 10 dB, $\nu_2 = \nu_1$ = 1. Hz, $2\sigma_1 = 2\sigma_2$ = .05 Hz $\tau_2 - \tau_1$ = 1.2 ms, T/2 (14,6) Equalizer, 4800 b/s, 10 dB ARQ Threshold

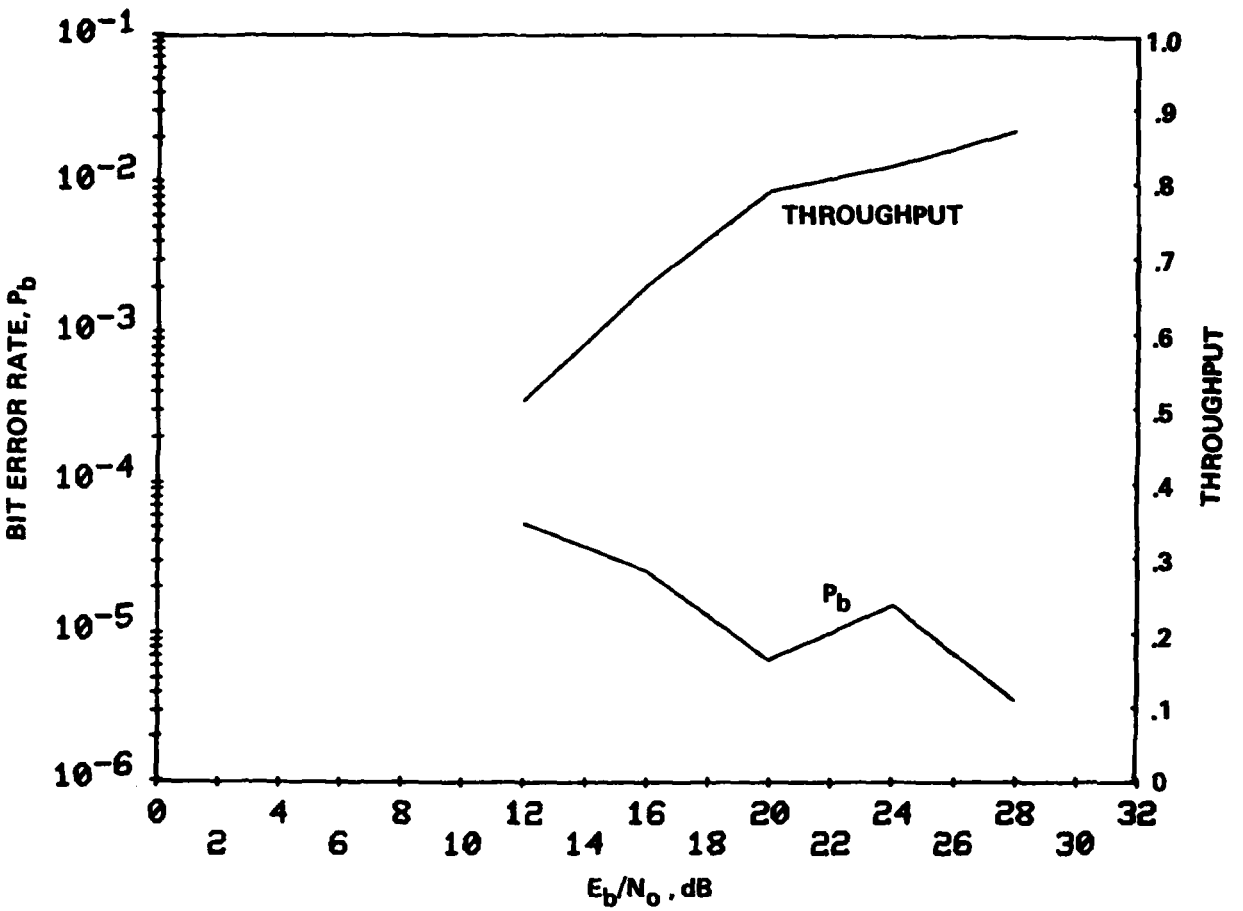


Figure 10-23. Bit Error Rate and Throughput versus Signal-to-Noise Ratio for $n=2$, $\overline{A}_1 = \overline{A}_2 = \infty$, $\tilde{A}_1 = 26$ dB, $\tilde{A}_2 = 10$ dB, $\nu_2 = -\nu_1 = 1.$ Hz, $2\sigma_1 = 2\sigma_2 = .1$ Hz, $\tau_2 - \tau_1 = 1.2$ ms, T/2 (14,6) Equalizer, 4800 b/s, 10 dB ARQ Threshold

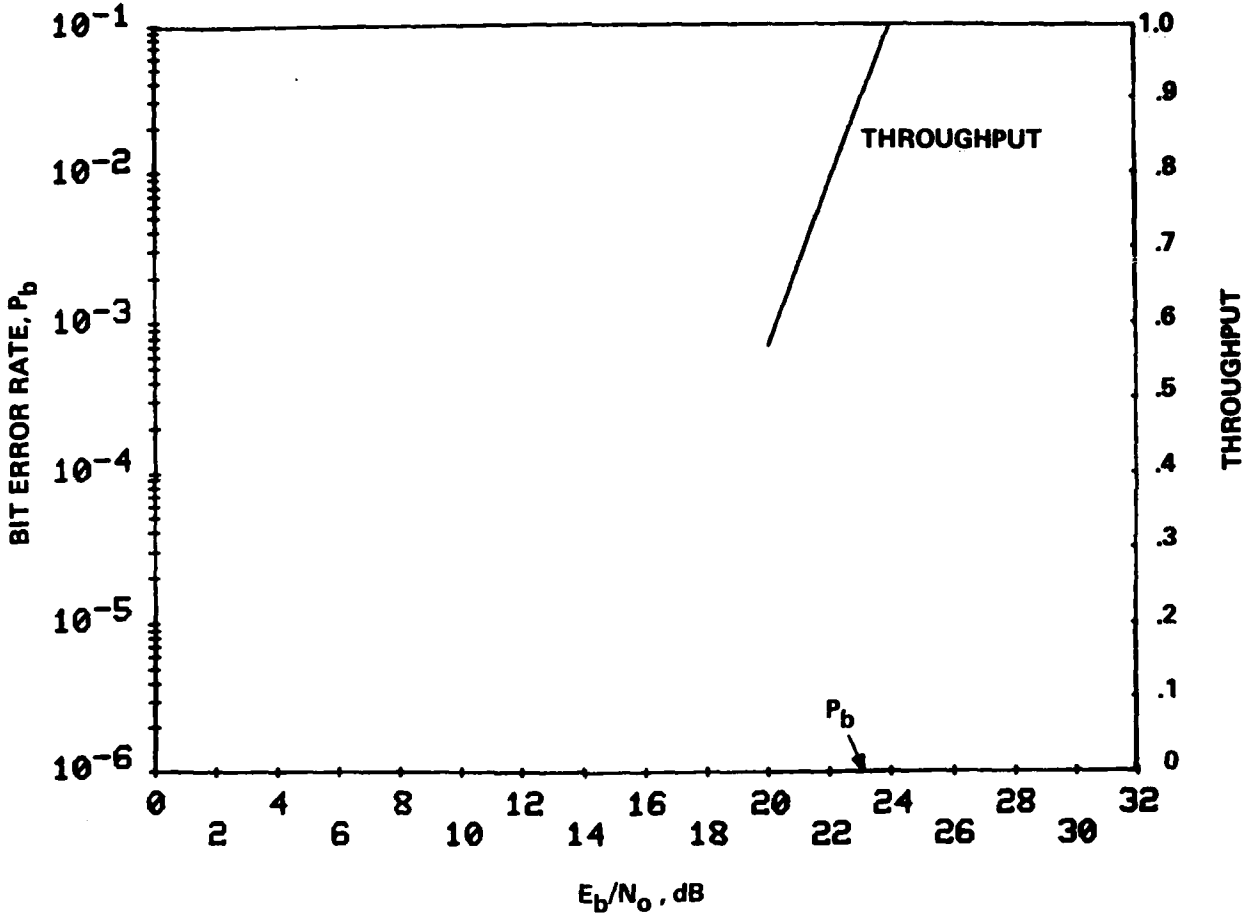


Figure 10-24. Bit Error Rate and Throughput versus Signal-to-Noise Ratio for n = 3, $\overline{A}_1 = \overline{A}_2 = \overline{A}_3 = \infty$, $\tilde{A}_1 = 24$ dB, $\tilde{A}_2 = 10$ dB, $\tilde{A}_3 = 12$ dB, $\nu_3 = -\nu_1 = .5$ Hz, $\nu_2 = 0$ Hz, $2\sigma_1 = 2\sigma_2 = 2\sigma_3 = .05$ Hz, $\tau_2 - \tau_1 = .6$ ms, $\tau_3 - \tau_1 = 2.8$ ms, T/2 (22,10) Equalizer, 2400 b/s, 10 dB ARQ Threshold

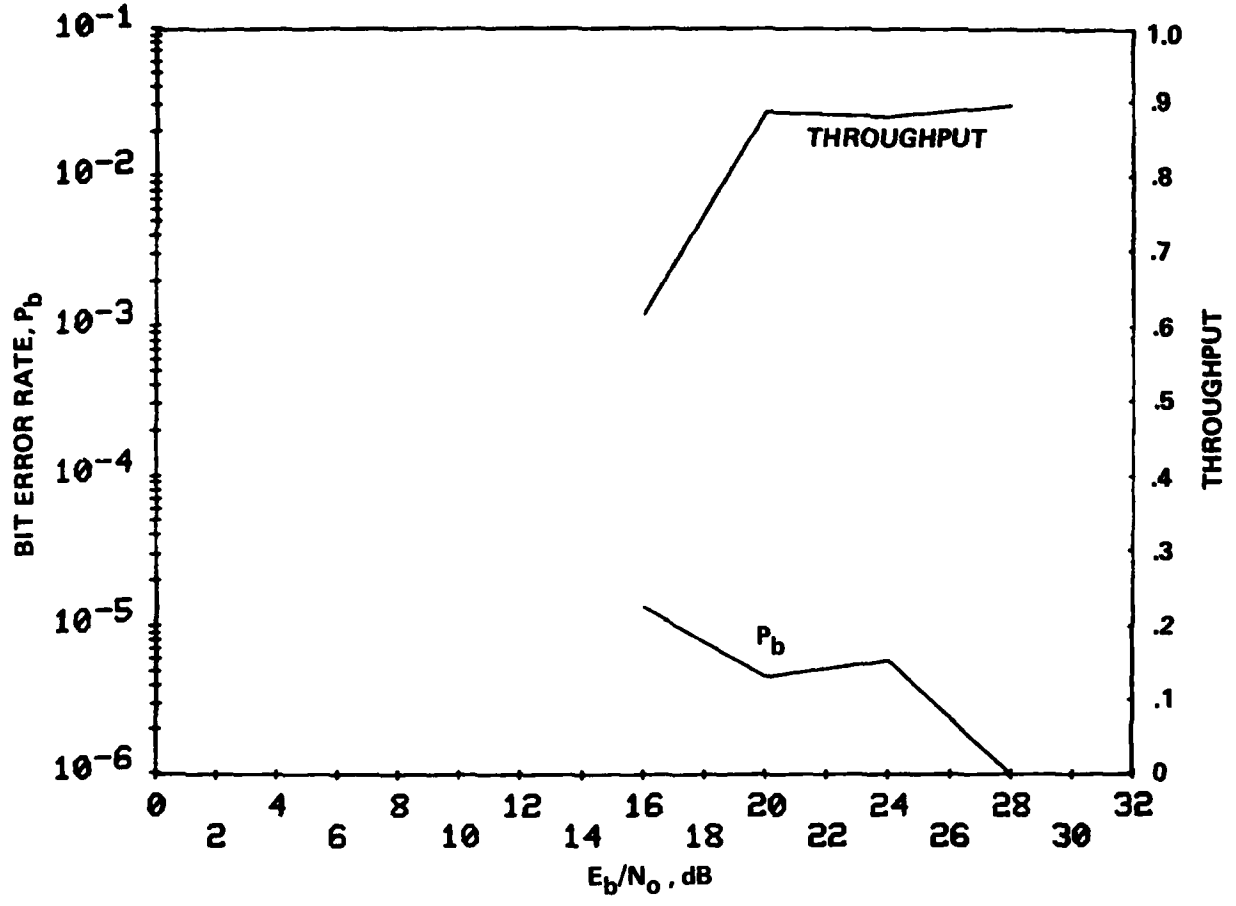


Figure 10-25. Bit Error Rate and Throughput versus Signal-to-Noise Ratio for n=3, $\overline{A}_1 = \overline{A}_2 = \overline{A}_3 = \infty$, $\tilde{A}_1$ = 24 dB, $\tilde{A}_2$ = 10 dB $\tilde{A}_3$ = 12 dB, $\nu_3 = -\nu_1$ = .5 Hz, ν_2 = 0 Hz, $2\sigma_1 = 2\sigma_2 = 2\sigma_3$ = .05 Hz, $\tau_2 - \tau_1$ = .6 ms, $\tau_3 - \tau_1$ = 2.8 ms, T/2 (22,10) Equalizer, 4800 b/s, 10 dB ARQ Threshold

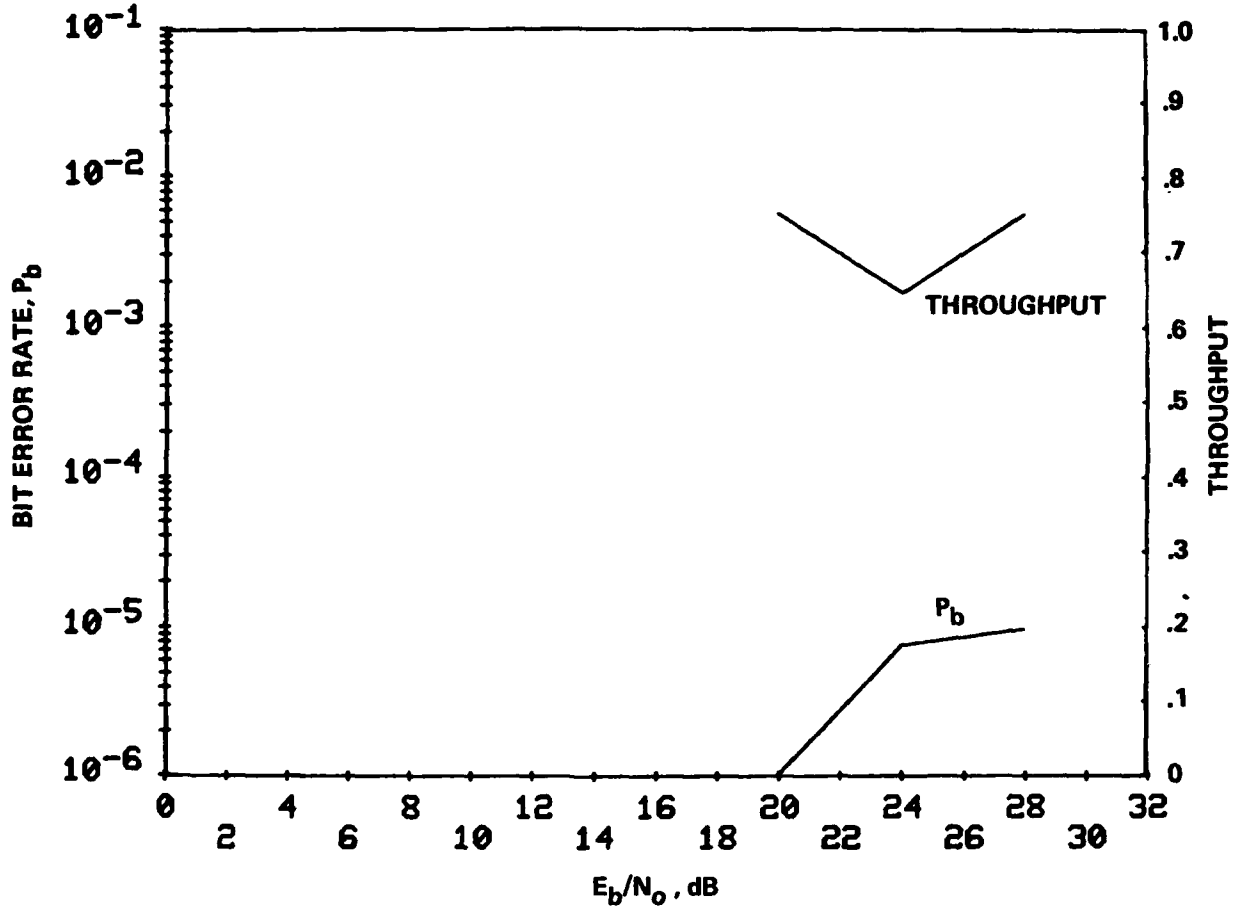


Figure 10-26. Bit Error Rate and Throughput versus Signal-to-Noise Ratio for n = 3, $\overline{A}_1 = \overline{A}_2 = \overline{A}_3 = \infty$, $\tilde{A}_1 = 24$ dB, $\tilde{A}_2 = 10$ dB, $\tilde{A}_3 = 12$ dB, $\nu_3 = -\nu_1 = .5$ Hz, $\nu_2 = 0$ Hz, $2\sigma_1 = 2\sigma_2 = 2\sigma_3 = .05$ Hz, $\tau_2 - \tau_1 = .6$ ms, $\tau_3 - \tau_1 = 2.8$ ms, T (11,10) Equalizer, 4800 b/s, 10 dB ARQ Threshold

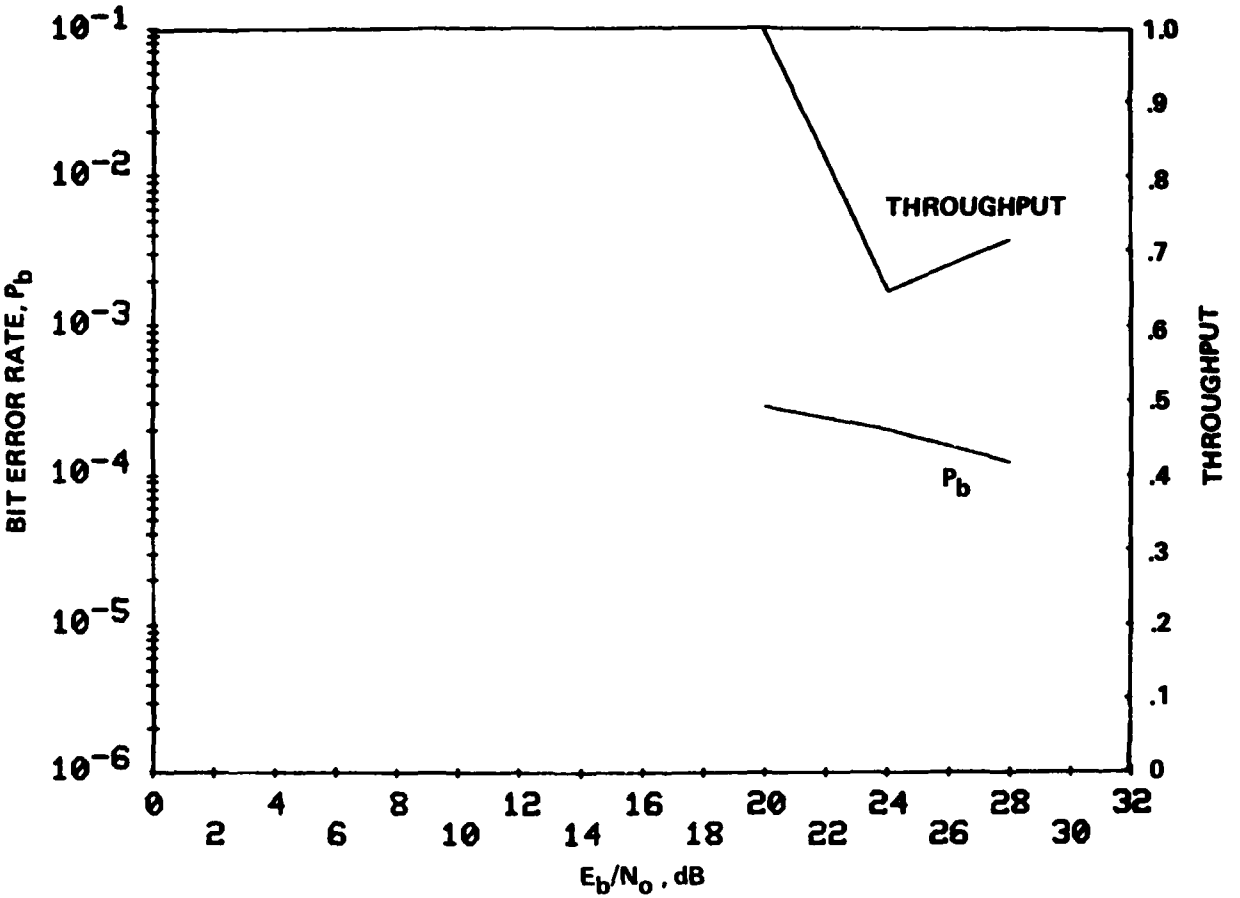


Figure 10-27. Bit Error Rate and Throughput versus Signal-to-Noise Ratio for n = 3, $\bar{A}_1 = \bar{A}_2 = \bar{A}_3$ = x, $\bar{A}_1$ = 24 dB, $\bar{A}_2$ = 10 dB, $\bar{A}_3$ = 12 dB, ν_3 = ν_1 = .5 Hz, ν_2 = 0 Hz, $2\sigma_1$ = $2\sigma_2$ = $2\sigma_3$ = .05 Hz, τ_2 τ_1 = .6 ms, τ_3 τ_1 = 2.8 ms, T/2 (22,10) Equalizer, 7200 b/s, 12 dB ARQ Threshold

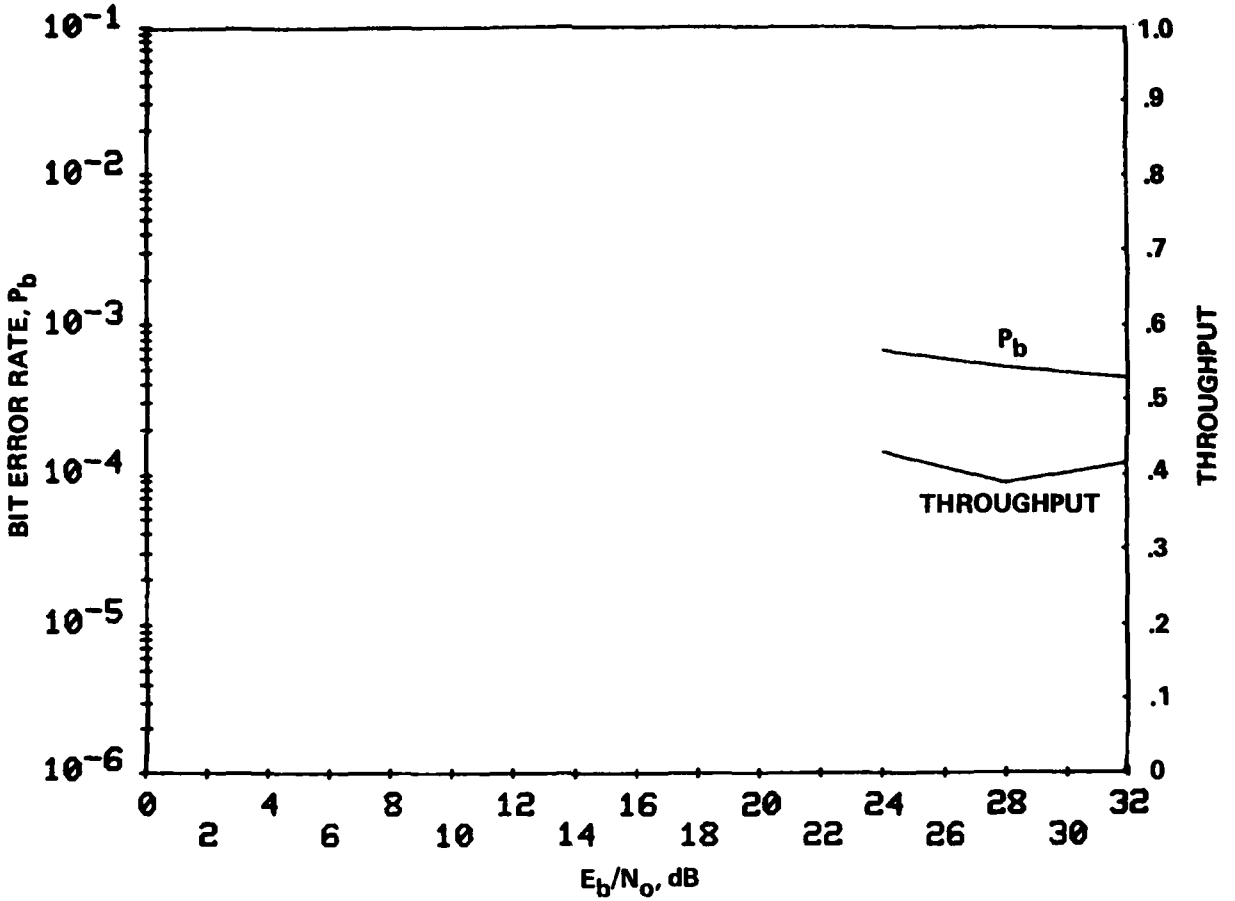


Figure 10-28. Bit Error Rate and Throughput versus Signal-to-Noise Ratio for $n=3$, $\overline{A}_1 = \overline{A}_2 = \overline{A}_3 = \infty$, $\tilde{A}_1 = 24$ dB, $\tilde{A}_2 = 10$ dB, $\tilde{A}_3 = 12$ dB, $\nu_3 = -\nu_1 = .5$ Hz, $\nu_2 = 0$ Hz, $2\sigma_1 = 2\sigma_2 = 2\sigma_3 = .05$ Hz, $\tau_2 - \tau_1 = .6$ ms, $\tau_3 - \tau_1 = 2.8$ ms, T/2 (22,10 Equalizer, 9600 b/s, 14 dB ARQ Threshold

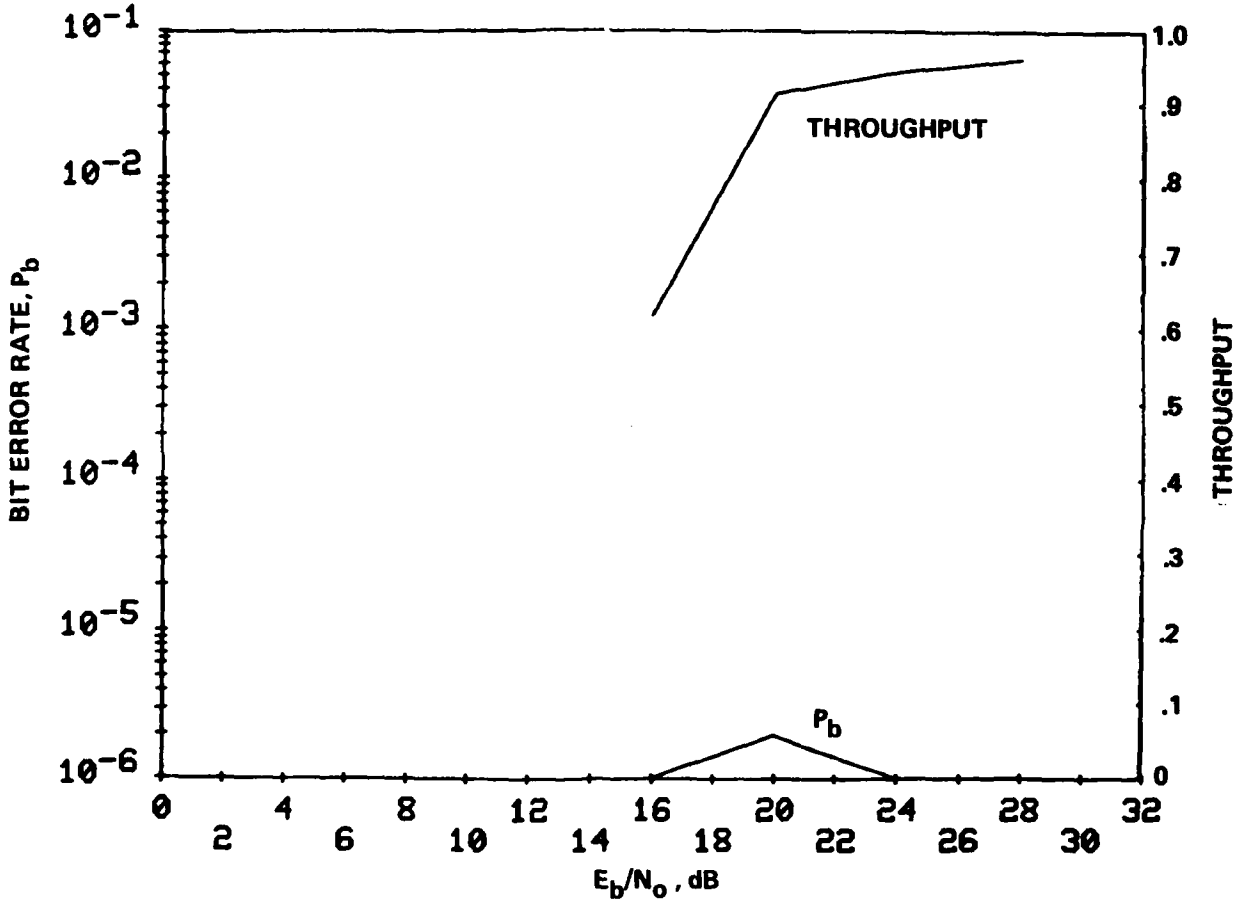


Figure 10-29. Bit Error Rate and Throughput versus Signal-to-Noise Ratio for n = 3, $\bar{A}_1 = \bar{A}_2 = \bar{A}_3 = \infty$, $\tilde{A}_1$ = 24 dB, $\tilde{A}_2$ = 10 dB, $\tilde{A}_3$ = 12 dB, $\nu_3 = -\nu_1 = 1.$ Hz, $\nu_2 = 0$ Hz, $2\sigma_1 = 2\sigma_2 = 2\sigma_3 = .05$ Hz, $\tau_2 - \tau_1 = .6$ ms, $\tau_3 - \tau_1 = 2.8$ ms, T/2 (22,10) Equalizer 4800 b/s, 10 dB ARQ Threshold

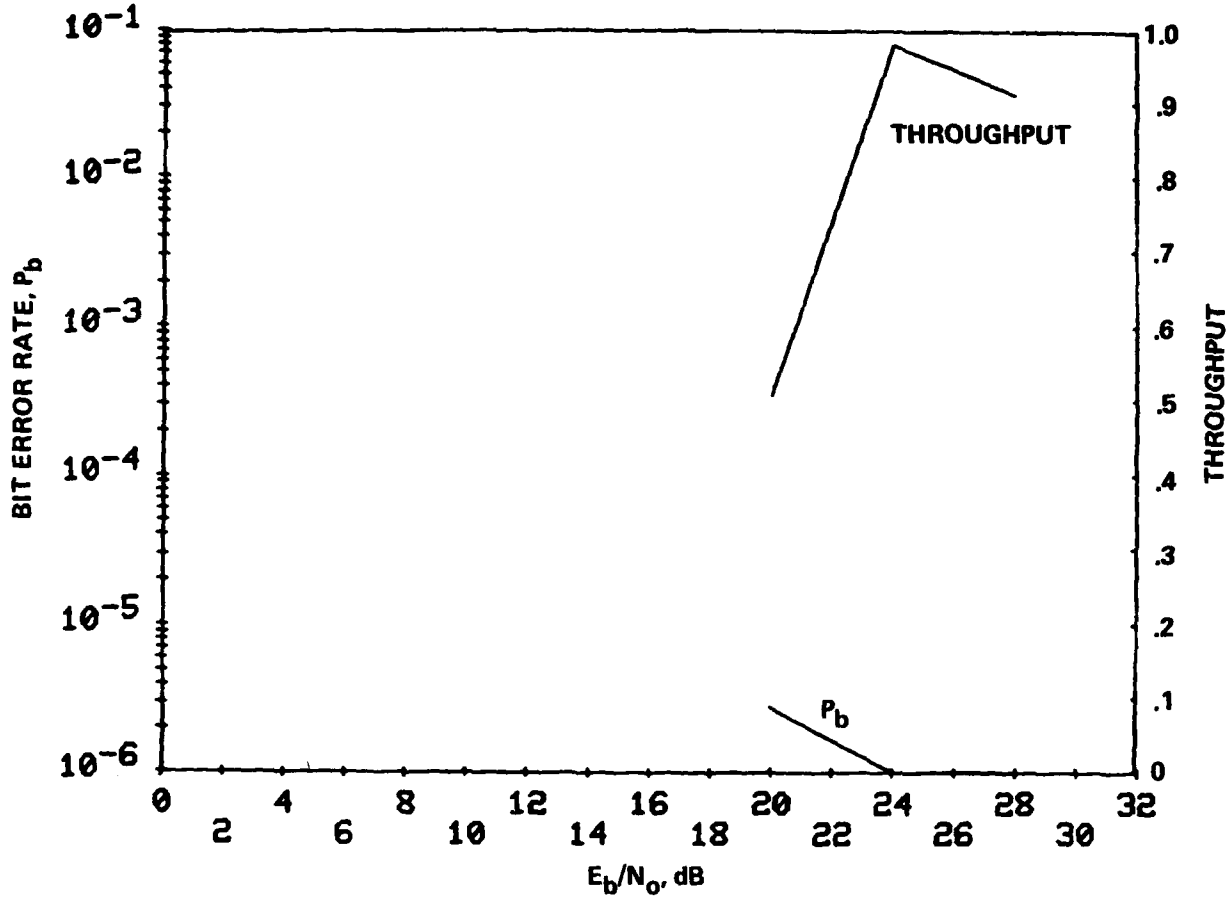


Figure 10-30. Bit Error Rate and Throughput versus Signal-to-Noise Ratio for n = 3, $\bar{A}_1 = \bar{A}_2 \approx \bar{A}_3 = \infty$, $\tilde{A}_1$ = 24 dB, $\tilde{A}_2$ = 10 dB, $\tilde{A}_3$ = 12 dB, $\nu_3 = -\nu_1$ = 1. Hz, ν_2 = 0 Hz, $2\sigma_1 = 2\sigma_2 = 2\sigma_3$ = .1 Hz, $\tau_2 - \tau_1$ = .6 ms, $\tau_3 - \tau_1$ = 2.8 ms, T/2 (22,10) Equalizer, 4800 b/s, 10 dB ARQ Threshold

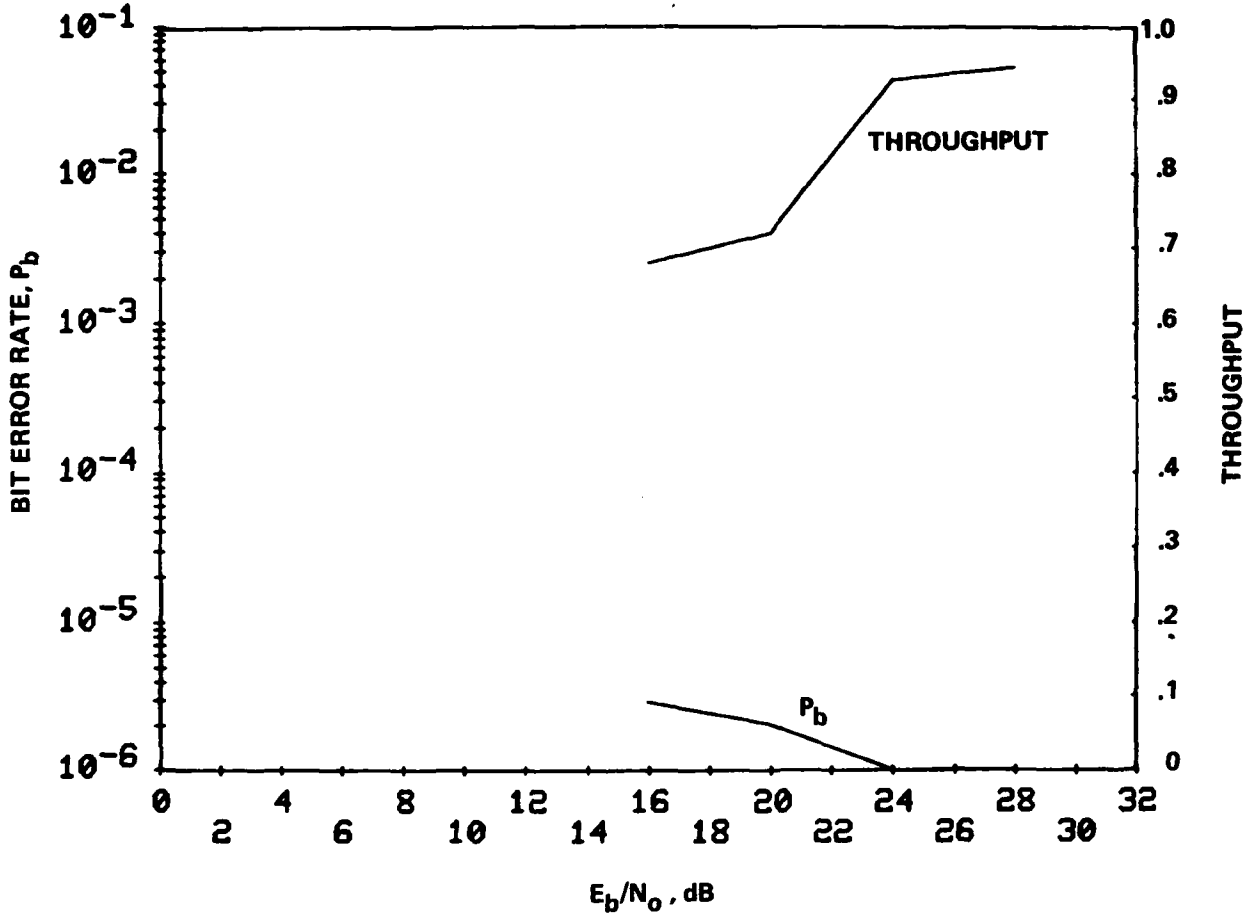


Figure 10-31. Bit Error Rate and Throughput versus Signal-to-Noise Ratio for n = 2, $\overline{A}_1 = \overline{A}_2 = \infty$, $\tilde{A}_1$ = 10 dB, $\tilde{A}_2$ = 20 dB, $\nu_2 = -\nu_1$ = .5 Hz, $2\sigma_1 = 2\sigma_2$ = .05 Hz, $\tau_2 - \tau_1$ = 5. ms, T (16,15) Equalizer, 4800 b/s, 10 dB ARQ Threshold

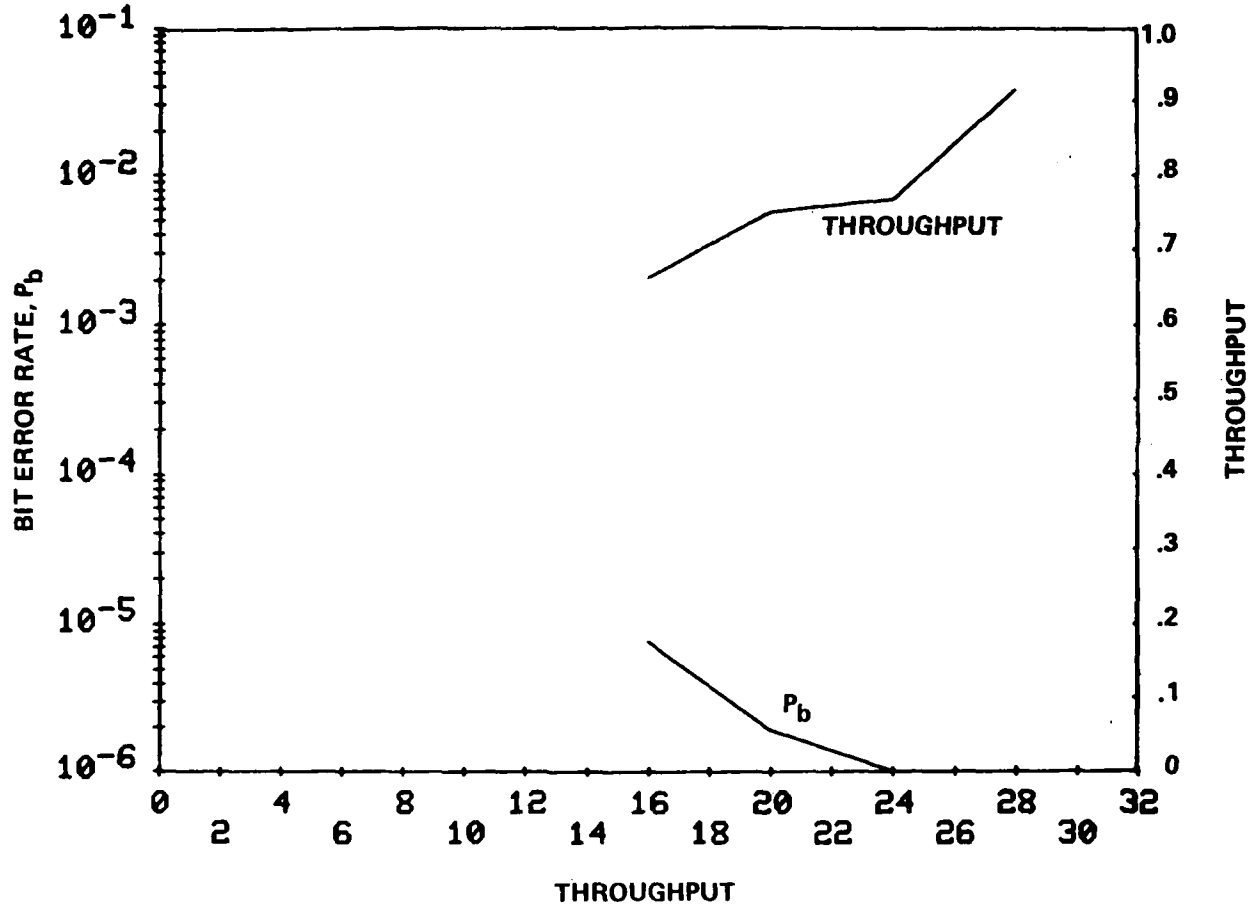


Figure 10-32. Bit Error Rate and Throughput versus Signal-to-Noise Ratio for n = 2, $\overline{A}_1 = \overline{A}_2 = \infty$, $\bar{A}_1$ = 10 dB, $\bar{A}_2$ = 20 dB, $\nu_2 = \nu_1$ = 1. Hz, $2\sigma_1 = 2\sigma_2$ = .05 Hz, $\tau_2 - \tau_1$ = 5. ms, T (16,15) Equalizer, 4800 b/s, 10 dB ARQ Threshold

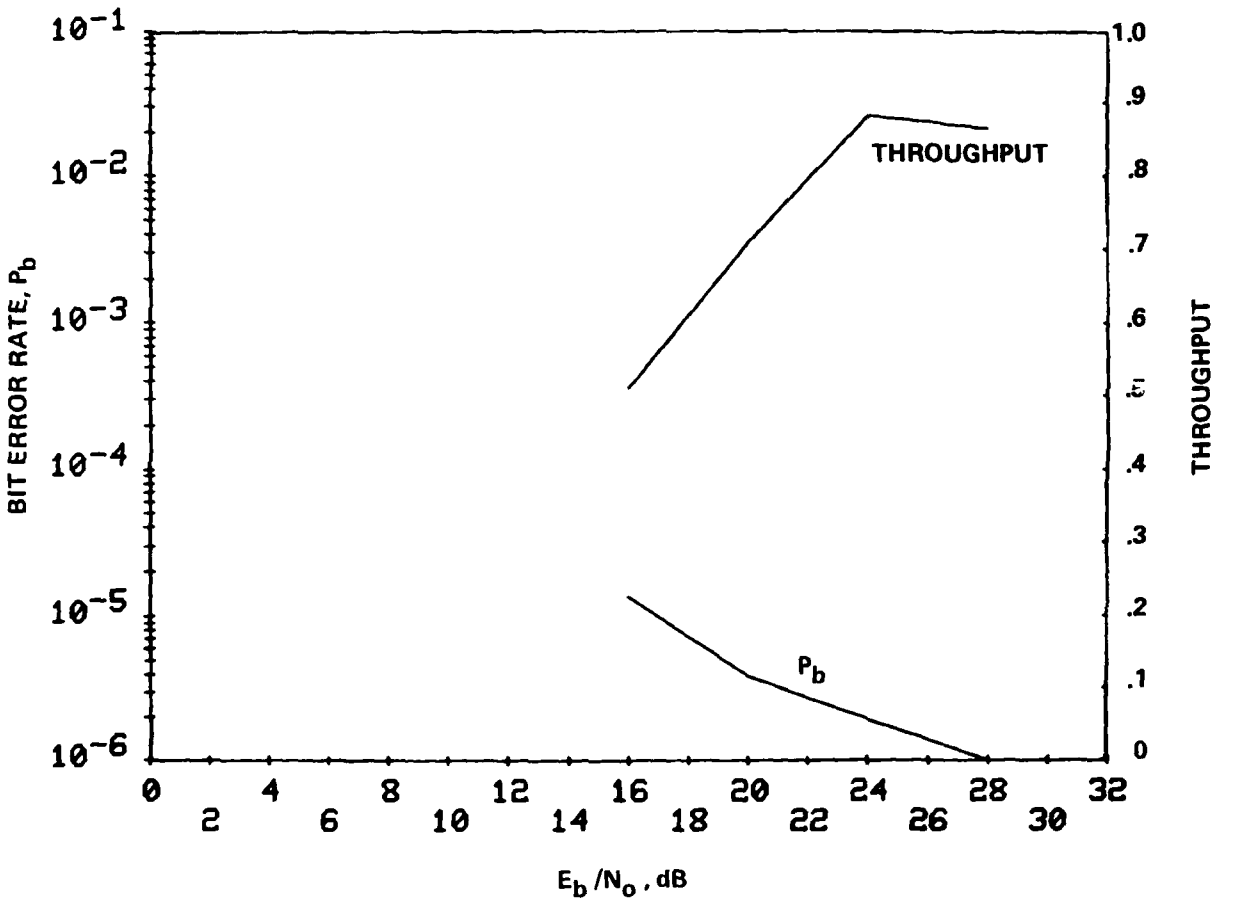


Figure 10-33. Bit Error Rate and Throughput versus Signal-to-Noise Ratio for n = 2, $\bar{A}_1 = \bar{A}_2 = \infty$, $\tilde{A}_1$ = 10 dB, $\tilde{A}_2$ = 20 dB, $\nu_2 = \nu_1 = 0$ Hz, $2\sigma_1 = 2\sigma_2 = .1$ Hz, $\tau_2 - \tau_1 = 5$. ms, T (16,15) Equalizer, 4800 b/s, 10 dB ARQ Threshold

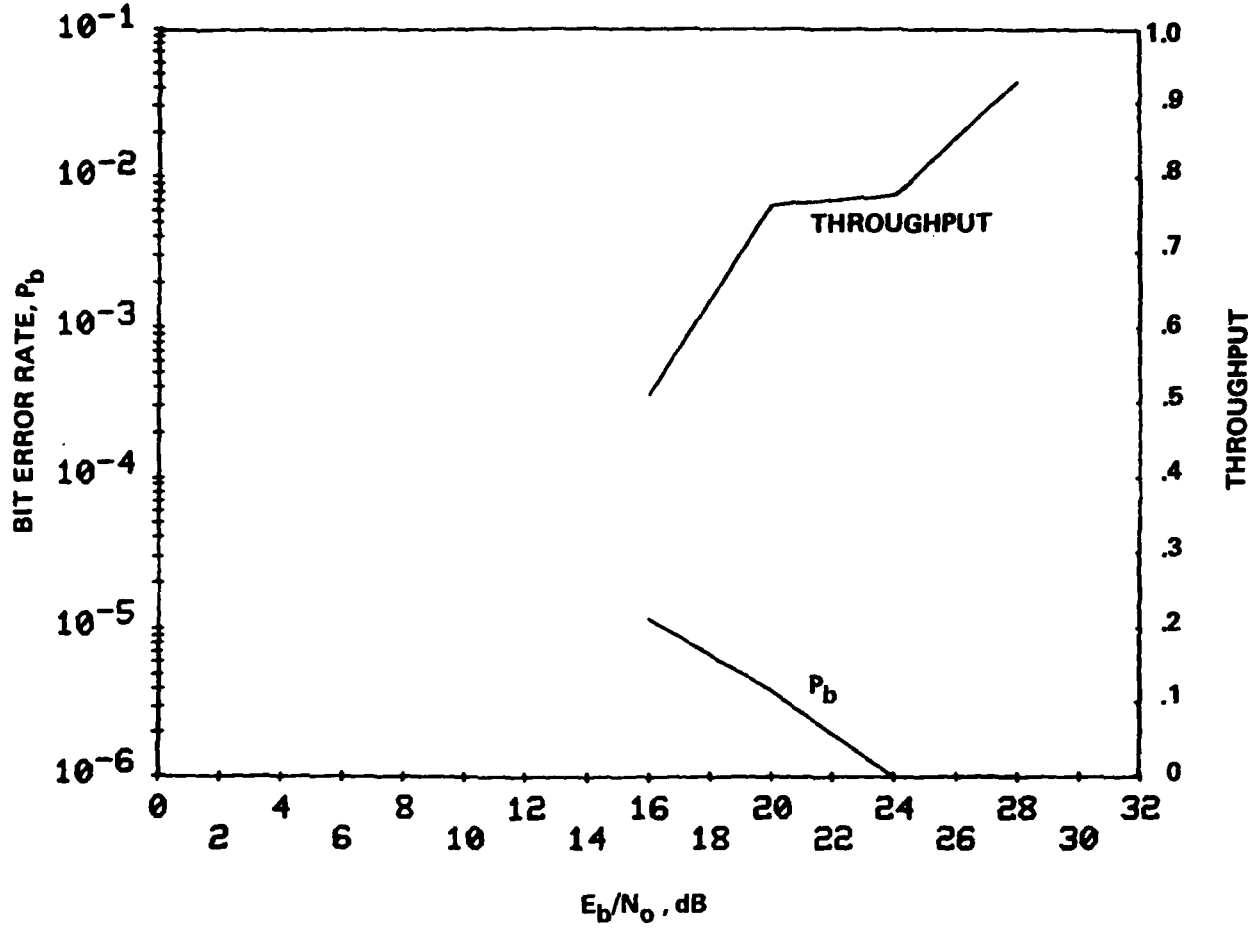


Figure 10-34. Bit Error Rate and Throughput versus Signal-to-Noise Ratio for n=2, $\overline{A}_1 = \overline{A}_2 = \infty$, $\hat{A}_1$ = 10 dB, $\hat{A}_2$ = 20 dB, $\nu_2 = -\nu_1$ = .25 Hz, $2\sigma_1 = 2\sigma_2$ = .1 Hz, $\tau_2 - \tau_1$ = 5. ms, T (16,15) Equalizer, 4800 b/s, 10 dB ARQ Threshold

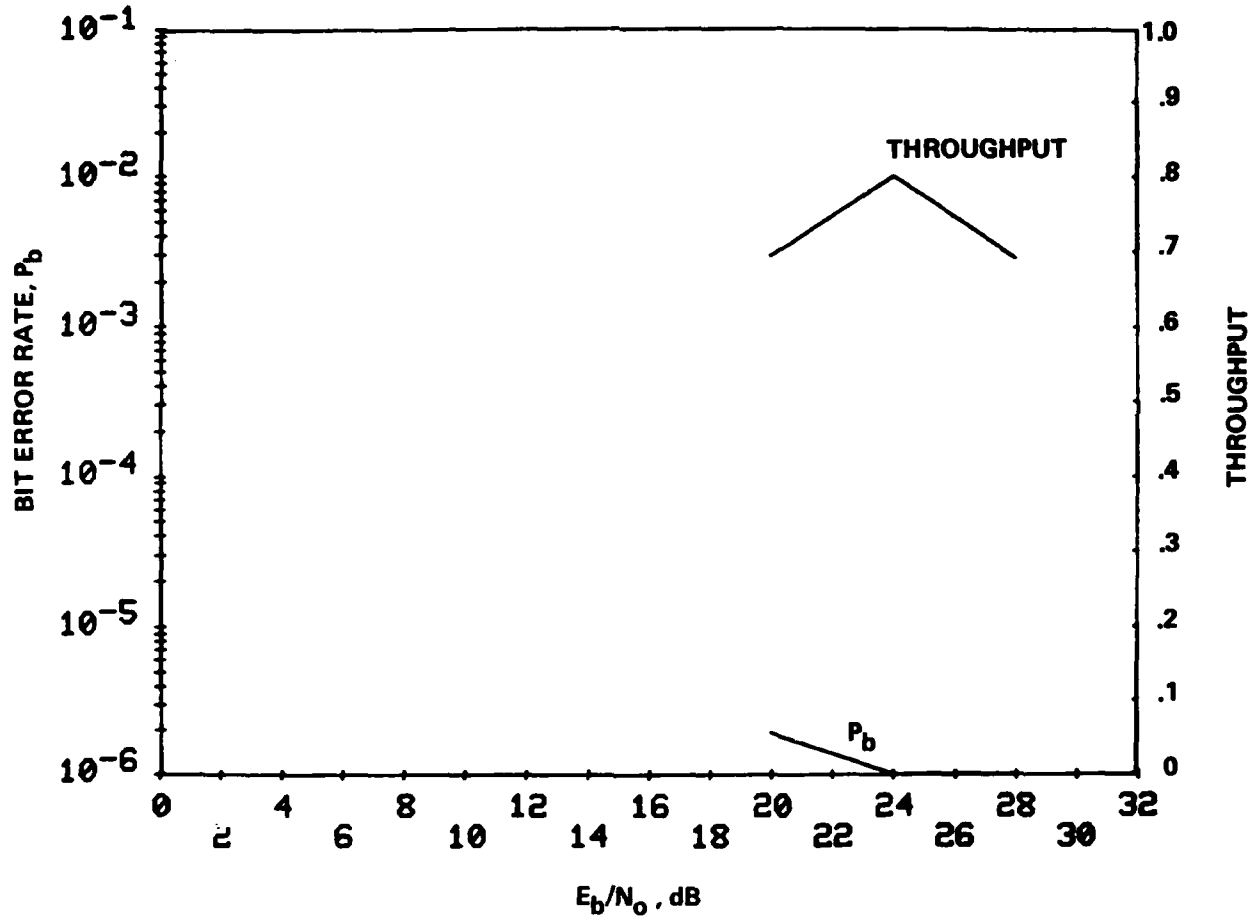


Figure 10-35. Bit Error Rate and Throughput versus Signal-to-Noise Ratio for n = 2, $\overline{A}_1 = \overline{A}_2 = \infty$, $\tilde{A}_1$ = 10 dB, $\tilde{A}_2$ = 20 dB, $\nu_2 = -\nu_1$ = .5 Hz, $2\sigma_1 = 2\sigma_2$ = .1 Hz, $\tau_2 - \tau_1$ = 5. ms, T (16,15) Equalizer, 4800 b/s, 10 dB ARQ Threshold

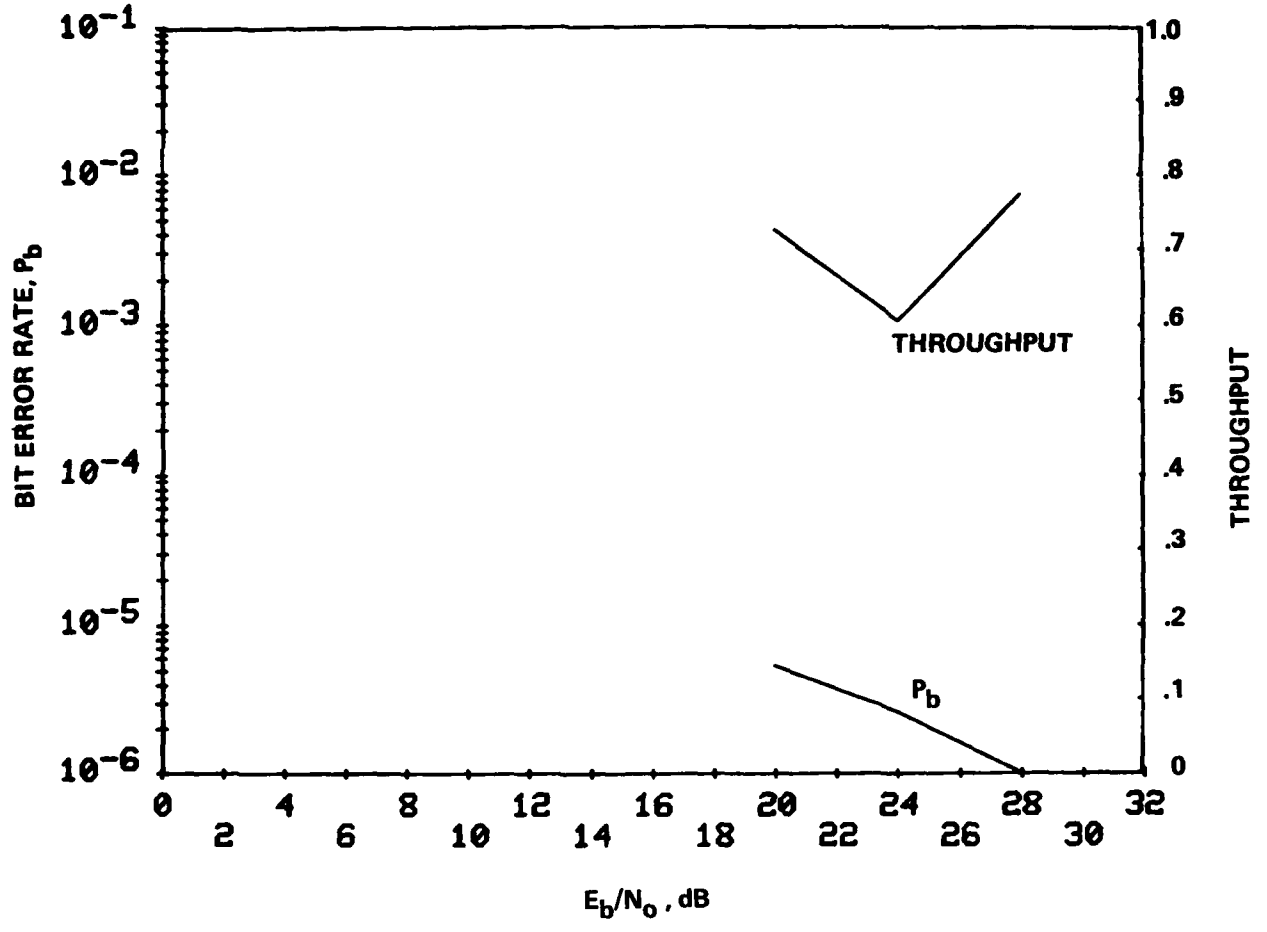


Figure 10-36. Bit Error Rate and Throughput versus Signal-to-Noise Ratio for $n=2$, $\overline{A}_1 = \overline{A}_2 = \infty$, $\tilde{A}_1 = 10$ dB, $\tilde{A}_2 = 20$ dB, $\nu_2 = -\nu_1 = 1.$ Hz, $2\sigma_1 = 2\sigma_2 = .1$ Hz, $\tau_2 - \tau_1 = 5.$ ms, T (16,15) Equalizer, 4800 b/s, 10 dB ARQ Threshold

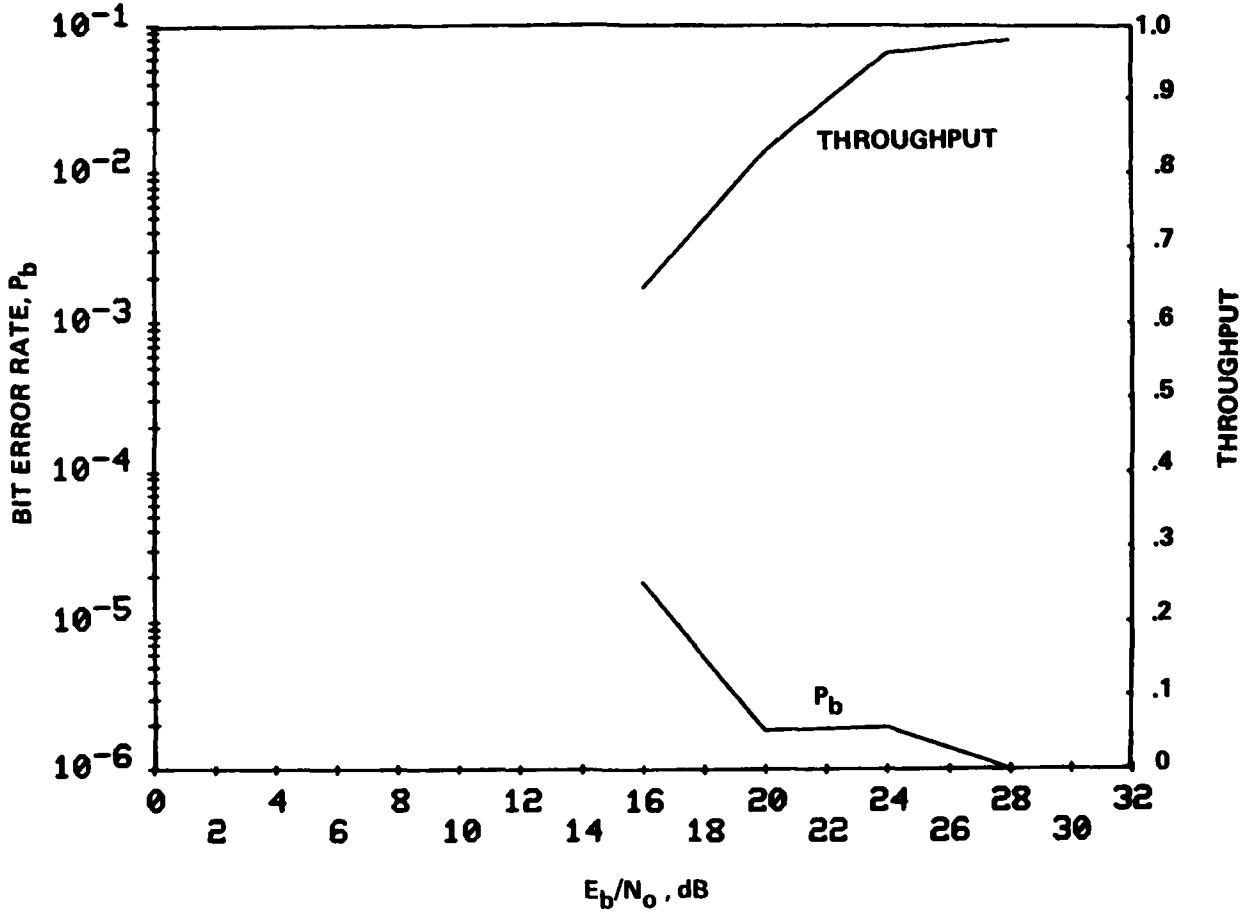


Figure 10-37. Bit Error Rate and Throughput versus Signal-to-Noise Ratio for n = 2, $\overline{A}_1 = \overline{A}_2 = \infty$, $\tilde{A}_1 = \tilde{A}_2 = 13$ dB, $\nu_2 - \nu_1 = 0$ Hz, $2\sigma_1 = 2\sigma_2 = .2$ Hz, $\tau_2 - \tau_1 = 1$. ms, T/2 (24,11) Equalizer, 4800 b/s, 10 dB ARQ Threshold

this curve was selected to correspond to that used for simulation results published on multitone modems [26]. On all of the figures, the error rate is plotted using the logarithmic scale on the left, and the throughput is plotted using the linear scale on the right. All figures except 10-19 through 10-21 plot performance in terms of bit error rate; the excepted curves show symbol error rate. The caption for each figure includes a channel description based on symbology used in the literature [26]:

- n = number of paths in channel
- $\bar{A}_i$ = decibel attenuation of the specular component on the i-th channel path
- $\tilde{A}_i$ = decibel attenuation of the Gaussian-scatter signal component on the i-th channel path
- υi = Doppler shift on the i-th channel path
- $2\sigma_i$ = frequency spread (fading rate) on the i-th channel path
- τi = delay on the i-th channel path

In addition to tests with the real-time channel simulator, the HFWBM equipment was briefly operated over a 24 km live link from Ava to Rome, N.Y. For this test operation, both HFWBM units remained at Rome, and the modulator output was sent over a microwave link to the HF transmit site at Ava. The HF receiver used at Rome was a Sunair Model GSR-920. The audio output from this receiver was applied as input to the HFWBM demodulator. Overall circuit quality (SNR, phase jitter) was measured using a 1 kHz tone from a HP4943A Transmission Impairment Measuring Set (TIMS). A chirp sounder was also operated from Ava to determine the skywave MUF and multipath spread. Table 10-4 lists the measurements recorded for the short live link test. A discussion and interpretation of these data, as well as all of the simulated channel results, is presented in the next section.

TABLE 10-4. PRELIMINARY LIVE LINK RESULTS

Ava to Rome N.Y., 10 Sept 1981, 9:00 – 12:00, MUF = 9.5 MHz

Frequency	SNR	Multipath	Phase Jitter	Data Rate	BER	Throughput
11.215 MHz	~30 dB	—	8.5°	2400	0.	100%
				4800	1.1×10^{-5}	99
				7200	2.8×10^{-3}	77
8.96	28-31	1.5 ms	8-10°	2400	0.	83
				4800	2.1×10^{-5}	NM
13.212	24-28	1.75	9-15°	2400	2.0×10^{-6}	71
5.869	20-26	1.75	10-16°	2400	6.1×10^{-5}	NM

10.3 Discussion and Interpretation of Results

The discussion and interpretation of results given here support the following conclusions:

- Reliable HF communications at data rates above 1 b/s/Hz are not only feasible, but have been demonstrated with real-time hardware
- Operation of the HFWBM in the ARQ mode is remarkably robust with respect to channel propagation conditions
- Nearly any desired error rate or throughput can be obtained by a simple adjustment of the ARQ threshold in the HFWBM (front panel thumbwheel switch)
- There does not appear to be any significant performance difference between T-spaced and T/2-spaced equalizers operating on fading channels
- The error rate performance of the single tone HFWBM operating at 4800 b/s is significantly better than published results for multitone modems operating at 2400 b/s
- Special combinations of multipath spread and high fade rates can lead to symbol synchronizer drift for two equal mean strength channel paths
- Operation of the HFWBM in the fixed percentage of training mode may be useful during good (high SNR) channel conditions, but ARQ operation is always preferred

- Operation at 9600 b/s over 3 kHz radio channels requires radio equipment having good phase stability.

The first two conclusions are readily apparent from the totality of performance data presented in Section 10.2. Theoretical performance benchmarks can be difficult to obtain for completely general fading channel conditions; however some comparisons with the available data are possible. For example, the single fading channel path results for curve No. 1 can be compared to the theoretical bit error rate curve for ideal coherent 4-phase PSK in slow Rayleigh fading. This comparison is shown in Figure 10-38. Note that since the theoretical results do not assume any error control, the HFWBM operating with its ARQ protocol performs better than ideal coherent PSK by about 2-1/2 orders of magnitude (in error rate). It is also interesting to refer back to Figure 10-3 to see that, for E_b/N_o greater than about 16 dB, this performance improvement is achieved at throughput values of 90 percent or more.

The robustness of the ARQ error control system can be observed by overlaying the error rate curves corresponding to a wide variety of channel conditions (using the same data rate). This has been done in Figure 10-39 which overlays the error rate results corresponding to curve Nos. 1, 2, 4, 6, 7, 12, 20, 23 and 29. These curves were selected because they represent the performance over channels with

- From 1 to 3 multipath components
- Fade rates from .05 to 2.0 Hz
- Multipath spreads from 0 to 5 ms
- Both equal and unequal mean path strengths (including non-minimum phase channels).

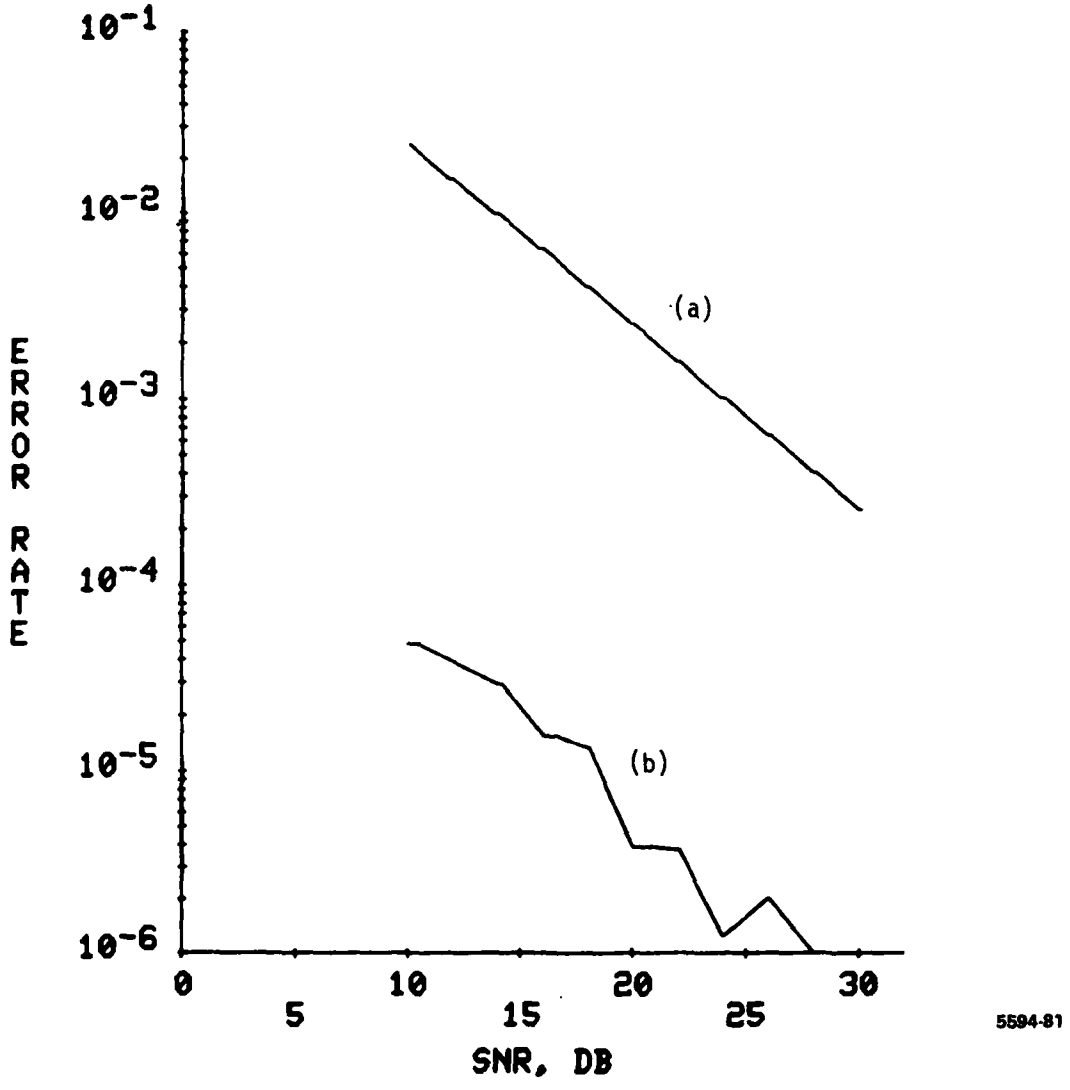


Figure 10-38. Bit Error Rate versus E_b/N_0 for 4-phase PSK in Slow Rayleigh Fading: (a) Ideal Coherent 40 PSK, (b) HFWBM with 40 DPSK and ARQ Error Control

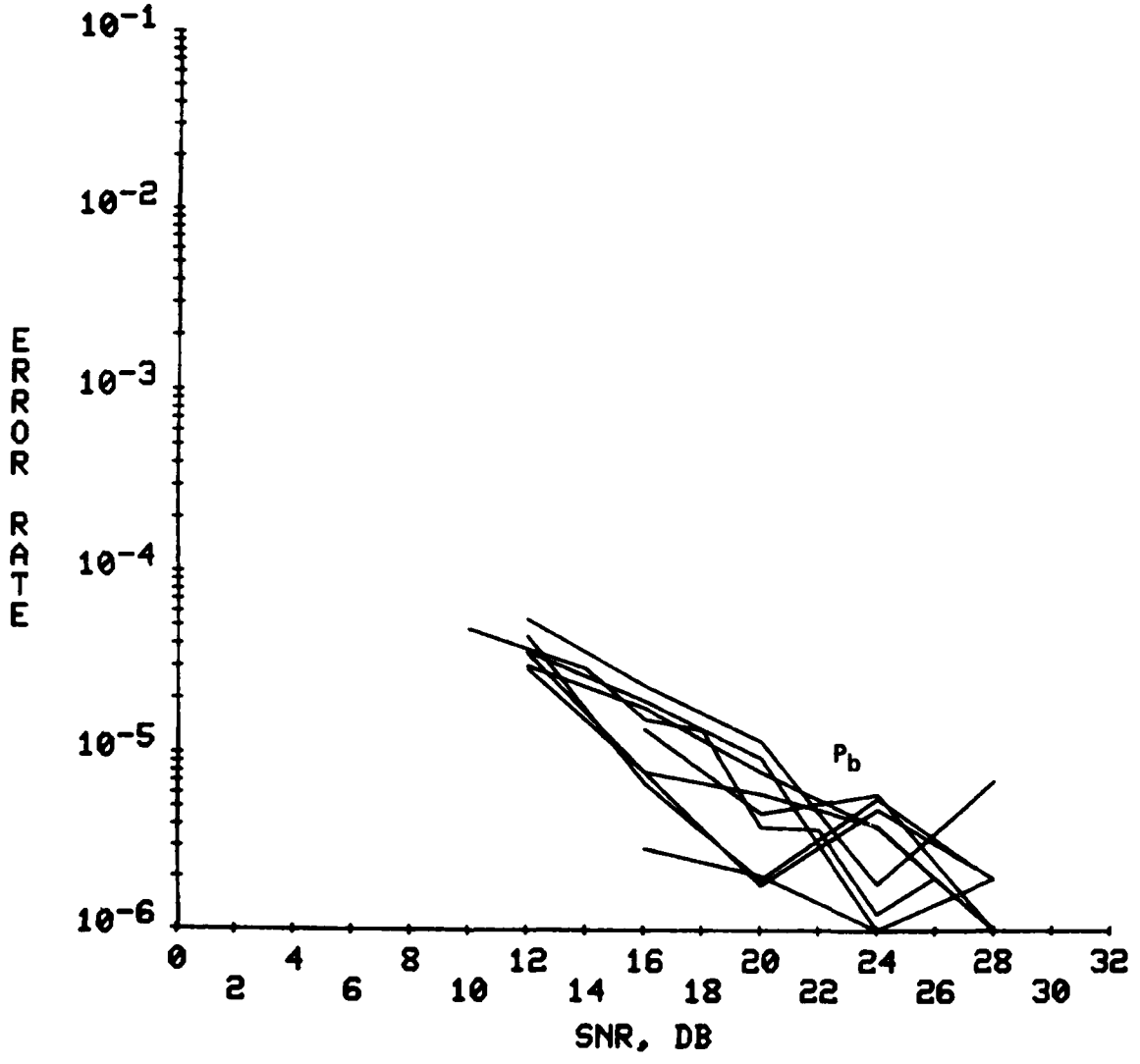


Figure 10-39. Overlay of Error Rate Data for Curve Nos. 1, 2, 4, 6, 7, 12, 20, 23, 29

It is rather remarkable that there is not a much wider scatter in the error rate performance over such a wide range of channel conditions.

The robustness may be ascribed to the ARQ operation. Once an SNR threshold is selected, the error rate will largely be confined to lie at or below what this SNR could support on a constant (nonfading) basis. Thus, as the channel changes, the error rate will remain relatively constant, while the throughput will change.* The ARQ threshold may be chosen to achieve nearly any desired error rate or throughput for a given fading channel. This can be seen by comparing the results for curve Nos. 11, 12 and 14. This comparison is highlighted in Figure 10-40 and 10-41. Figure 10-40 shows how the error rate can be controlled for the given channel conditions by selecting 8, 10 or 12 dB ARQ thresholds. Inasmuch as ideal conditions of low error rate and high throughput place conflicting requirements on threshold selection, these data demonstrate the utility of the HFWBM front panel threshold (thumbwheel) selector to conveniently effect the desired trade-off for the application at hand.

The absence of any significant performance difference between T-spaced and T/2-spaced equalizers operating on fading channels is a bit of a surprise. A superiority of T/2 spacing had been conjectured because of its relative immunity to offset in symbol synchronization phase (see Section 4.2.2). The absence of any significant performance difference is observed by pairwise comparison of the results corresponding to curve Nos. 5,6; 12,13; and 23,24. A possible explanation is that the passband timing technique is doing a good

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*This effect is in contrast with a forward error correction (FEC) coding system where the throughput is fixed and the error rate can vary.

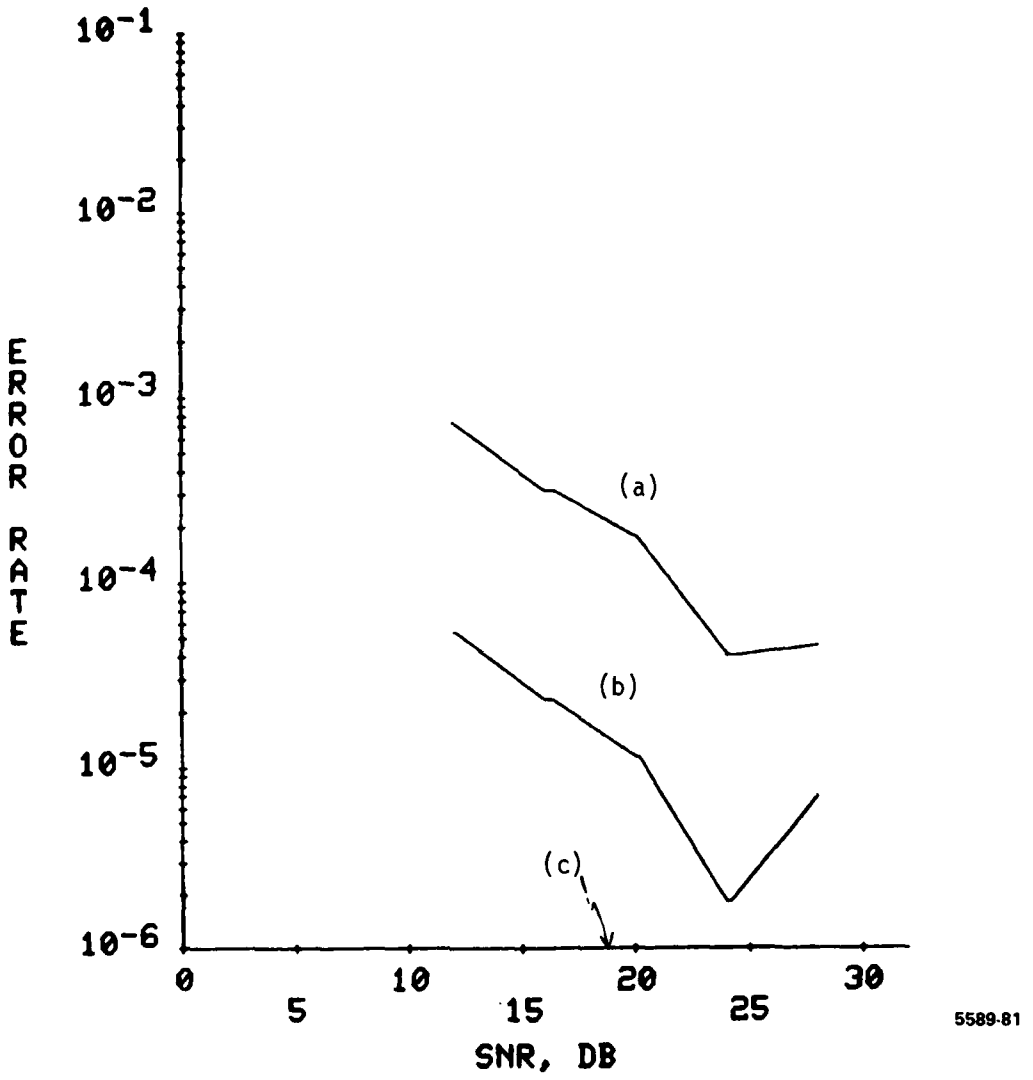

Figure 10-40. Measured Bit Error Rate versus E_b/N_0 for 4800 b/s in 2-path Fading Channel: $\tilde{A}_1$ = 26 dB, $\tilde{A}_2$ = 10 dB, τ_1 = 0, τ_2 = .4 ms, ν_1 = −.5 Hz, ν_2 = .5 Hz, $2\sigma_1 = 2\sigma_2$ = .05 Hz; T/2 (14,6) DFE. ARQ Thresholds: (a) 8 dB, (b) 10 dB, (c) 12 dB

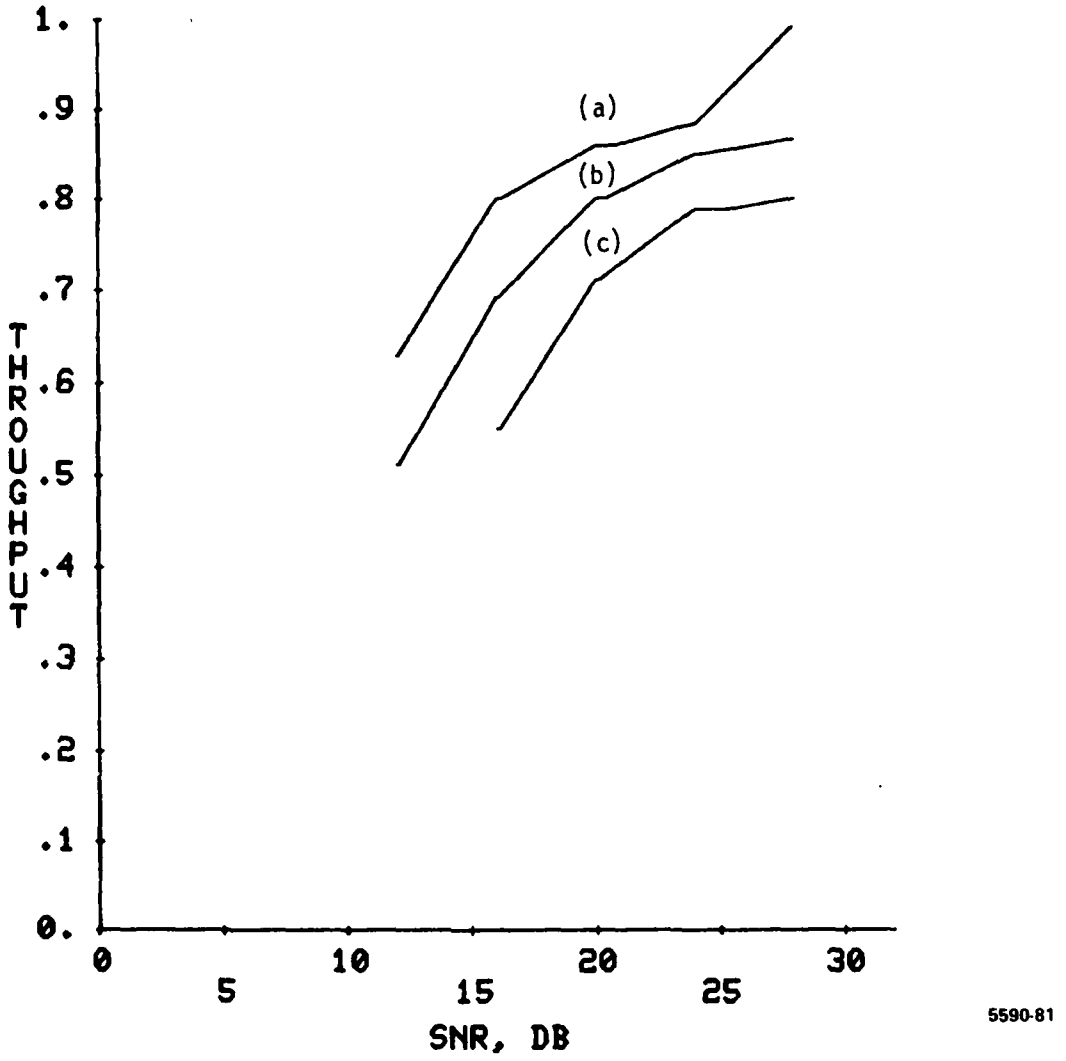

Figure 10-41. Measured Throughput versus E_b/N_o Corresponding to Data in Figure 10-40: (a) 8 dB ARQ Threshold, (b) 10 dB ARQ Threshold, (c) 12 dB ARQ Threshold

job of continuously optimizing the sampling phase for the fading multipath channel conditions studied. A second possibility is that the T/2-spaced equalizer, which requires more taps, introduces larger self-noise which offsets any performance gain. There is not yet enough data to prove either hypothesis, so the conclusion is a tentative one. There is a hint of some anomalous behavior starting to appear in the case of the T-spaced equalizer results corresponding to curve No. 24 (see Figure 10-26). More data should be taken to compare T versus T/2 equalizer performance on fading channels. If the tentative conclusion reached here is verified, the capabilities of the HFWBM equipment to handle multipath spreads of greater than 5 ms. (using T-spacing) could prove very useful when such conditions exist.

Figure 10-41 shows a comparison between the HFWBM results corresponding to curve No. 35 and published results for the AN/USC-10 and AN/ACQ-6 multitone modems operating under the same simulated channel conditions [26]. Note that the HFWBM equipment was operated at a nominal 4800 b/s rate while the multitone modems operate at a fixed 2400 b/s rate. The bit error rate of the HFWBM is observed to be three orders of magnitude lower than the multitone modems. Referring back to Figure 10-37, the throughput of the HFWBM is also observed to be well above the 50 percent level that would correspond to a true 2400 b/s information rate. In fact, the throughput is greater than 83 percent and 96 percent for signal-to-noise ratios greater than 20 dB and 24 dB (E_b/N_o), respectively. Note also that the abscissa in both figures is mean SNR, and that a comparison on the basis of peak SNR would show the relative performance of the single tone HFWBM in even more favorable terms vis-a-vis the multitone modems.

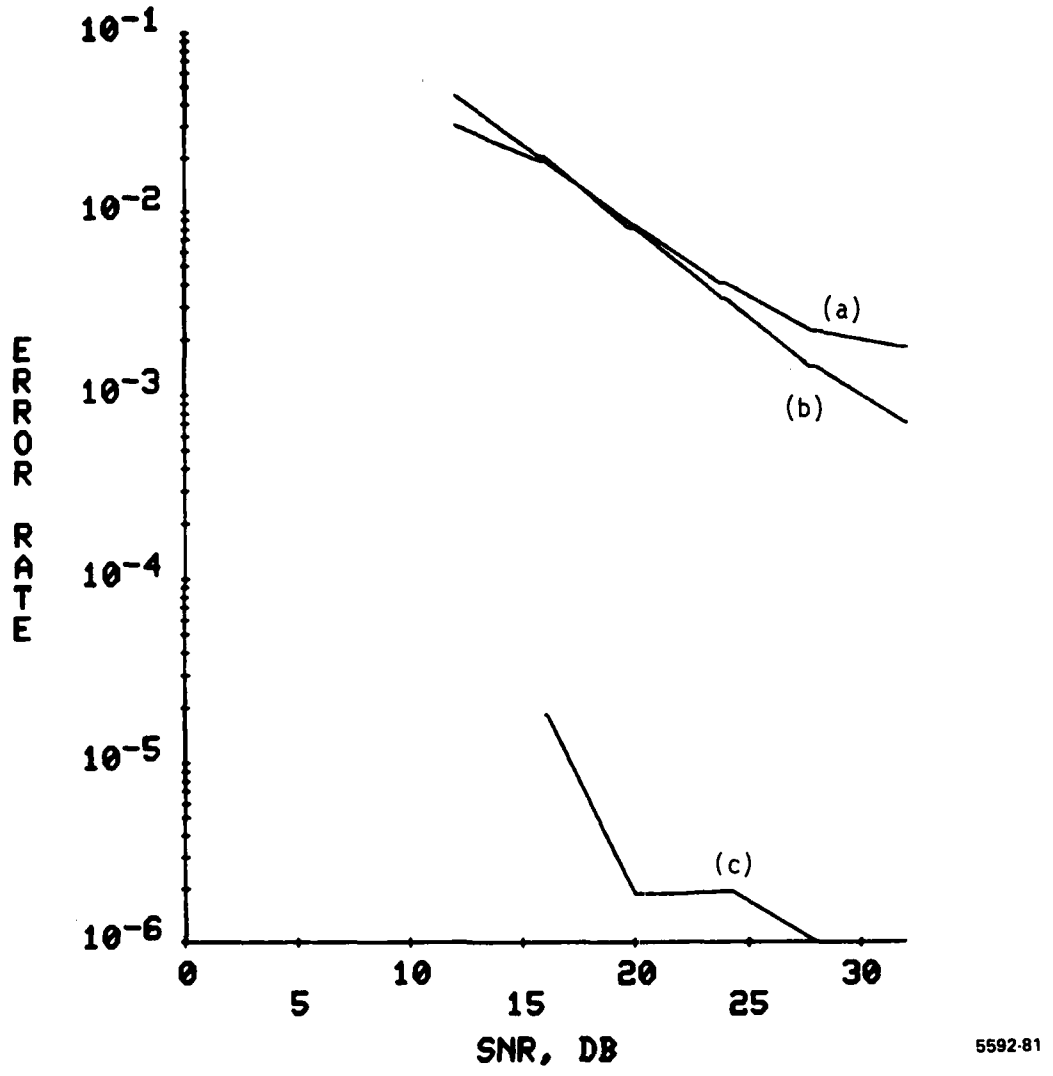

Figure 10-42. Measured Bit Error Rates vs. E_b/N_0 for 2-path Fading Channel: $\tilde{A}_1 = \tilde{A}_2 = 13$ dB. $\tau_2 - \tau_1 = 1.0$ ms, $\nu_1 = \nu_2 = 0$ Hz, $2\sigma_1 = 2\sigma_2 = .2$ Hz. (a) USC-10 2400 bps Modem. (b) ACQ-6 2400 bps Modem, (c) HFWBM at 4800 bps

Attempts to obtain similar performance comparisons at higher fade rates (e.g., $2_1 = 2_2 = 1.0$ Hz) at the DICEF facility were unsuccessful. Initial indications suggested this was due to slips in the symbol synchronizer. Subsequent tests conducted at GTE confirmed this as the problem and further showed that it tended to occur only when two equal mean strength paths were separated by an odd multiple of T/2 (half the symbol interval). Performance at other multipath delay separations did not exhibit this problem, even at high fade rates. Steps taken to minimize the problem in the final firmware included the following.

- Symmetric rounding and double precision arithmetic were introduced in certain critical portions of the synchronizer phase locked loop (PLL)
- The effective bandwidth of the PLL was narrowed
- The PLL was changed from a second-order to a first-order characteristic.

These modifications significantly improved operation in the special channel cases without deleterious effect on prior test results. It is recommended, however, that a closer analytical study be conducted to determine the reasons for synchronizer sensitivity to particular channel conditions.

The curves for the fixed-percent training mode (Nos. 17, 18 and 19) indicate significantly poorer performance than that obtained when operating in the ARQ mode under identical channel conditions (see results corresponding to curves 11, 12 or 14 for comparison). At low SNR, part of the explanation lies in the equalizer hang-up problem reported in Section 9. Without ARQ, there is nothing to prevent the instantaneous symbol SNR from dropping below 10 dB

during periods of decision-directed equalizer adaptation. This event, which was observed to promote equalizer hang-up, can occur on fading channels even before the mean SNR is as low as 10 dB. For example, the data given in Section 3.1 shows that the instantaneous SNR on a Rayleigh fading channel will fade below 10 dB with probability 0.07 when the mean SNR is 20 dB; the probability of the event increases to 0.2 when the mean channel SNR is 15 dB. A train-and-freeze option was added to help this problem. Although this may be of benefit on very slowly fading channels, more rapidly varying conditions still require continuous equalizer adaptation.

A further problem with fixed percent training is that the equalizer will not always receive training as soon as it needs it, and that it will often receive training when it is not needed (i.e., when decision directed adaptation is adequate). Demodulated data will be passed to the terminal equipment even when the channel is known to be poor. All of these facts support the observed results which show fixed percent training to be generally inferior to ARQ operation in both error rate and throughput. Comparison of Figures 10-19 and 10-20 shows the expected improvement in error rate as fixed training is increased from 12.5 to 25 percent. By further comparison with the results of Figure 10-21 it can be concluded that, for this particular channel, there is no apparent advantage in increasing the fixed training from 25 to 50 percent. Figure 10-20 and 10-21 do show a continuing reduction in error rate with increasing SNR, suggesting fixed percent training may constitute a reasonable fall-back mode of operation when the mean channel SNR is high and a return link to support the ARQ protocol is not available.

The preliminary live link test results presented in Table 10-4 provide a check that the HFWBM will interface with and operate successfuly through

on-the-air HF radio equipment. The results at 11.215 MHz represent primarily groundwave measurements which serve as a baseline for evaluating the adequacy of the equipment. No measurements were taken with this equipment at 9600 b/s. Note that the RMS phase jitter on a 1 kHz tone was measured to be 8.5^{o}. The HF receiver used for these tests is believed to be the most significant contributor to this jitter. This amount of jitter effectively precludes testing at 9600 b/s where 16-phase keying results in decision boundaries at $\pm 11.25^{o}$. It is recommended that a receiver with better phase stability be used in subsequent live link tests.

A chirp sounder was operated from the transmit site at Ava, N.Y., during these tests to measure the MUF and multipath indicated in Table 10-4. There were occasions when the sounder swept through the band being used for the HFWBM tests, with no noticeable accumulation of error counts. This "accidental testing" indicates some robustness of the HFWBM to narrowband co-channel interference, although no other tests were performed to explore this issue further. Such tests could be of considerable interest.

11.0 CONCLUSIONS

This project has developed two identical high data rate HF modem (HFWBM) terminals which offer reliable data communication at rates above 1 b/s/Hz over practical HF radio circuits. The characteristics and performance of the HFWBM have been shown to meet or exceed all contract specifications. In the contract SOW, operation at 2400 b/s and 4800 b/s were requirements, while operation at 9600 b/s in a 3 kHz channel was stated as a design goal. The HFWBM has been demonstrated to be capable of sustaining rates of 2400 b/s, 4800 b/s, 7200 b/s and 9600 b/s in 3 kHz channels.

A square-root Kalman equalizer adaptation algorithm has been shown to have the tracking agility and stability characteristics required to successfully follow the time-varying HF channel. Designed with an integral automatic-repeat-request (ARQ) system, the HFWBM operating in this mode achieves very low error rate, high throughput, and is remarkably robust with respect to channel conditions. Other significant conclusions which are supported by evidence in the main body of the report include the following:

- Nearly any desired error rate or throughput can be obtained by a simple adjustment of the ARQ threshold in the HFWBM (front panel thumbwheel switch)
- There does not appear to be any significant performance difference between T-spaced and T/2-spaced equalizers operating on fading channels
- The error rate performance of the single tone HFWBM operating at 4800 b/s is significantly better than published results for multitone modems operating at 2400 b/s

- Special combinations of multipath spread and high fade rates can lead to symbol synchronizer drift for two equal mean strength channel paths

- Operation of the HFWBM in the fixed percentage of training mode may be useful during good (high SNR) channel conditions, but ARQ operation is always preferred

- Operation at 9600 b/s over 3 kHz radio channels requires radio equipment having good phase stability.

Recommendations for further testing and suggested modem improvements are given in the next section.

12.0 RECOMMENDATIONS

Below is a list of recommendations for future testing and development of the HFWBM equipment. The basis or reason for each recommendation is briefly given along with a reference to the main body of this report where more information may be found.

	Recommendation	Reason/Basis
1.	Conduct long-haul live link tests	• Only short link data currently available (see Section 10.2)
2.	Use ARQ as primary test mode	• HFWBM specifically designed for ARQ operation; achieves best performance in this mode (see Section 10.3)
3.	Use high quality receiver having good phase stability	• Needed for high data rate operation (see Section 10.3)
4.	Explore techniques for automatic adaptation of equalizer size	• Optimize performance (see Section 9.0)
5.	Explore solutions to equalize hang-up	• Would allow operation below 10 dB SNR (see Section 9.0)
6.	Write an O&M manual for the HFWBM	• Would provide more complete documentation on equipment and features (see Section 8)
7.	Analyze symbol synchronizer operation for special channel cases	• Could lead to improved performance on special channels (see Section 10.3)

Recommendation	Reason/Basis
8. Test against co-channel interference	• Would provide additional useful performance data (see Section 10.3)
9. Design and implement elastic buffering scheme for ARQ operation	• Would provide constant throughput (see Section 10.3)

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APPENDIX A

RAW MEASUREMENT DATA

The following pages represent a listing of the ASCII file containing the raw measurement data from the DICEF tests. The format of this file is as follows:

```
I
N
EBNO, ERRS, NB, RS, NS, NQ, NR                    $ Comment
.
.
.
EBNO, ERRS, NB, RS, NS, NQ, NR                    $ Comment
```

(N lines)

where

I = Curve No.
N = Number of data points for this curve
EBNO = Signal-to-Noise Ratio per Bit (E_b/N_o), in dB
ERRS = { Bit error count (BE), for all curves except 17-19 ; Symbol error count (SE), for curves 17-19 }
NB = Information bit count, in thousands (000s)
RS = Total received symbol count, in hundreds (00s)
NS = Output information symbol count, in hundreds (00s)
NQ = Total ARQ count
NR = ARQ retry count
$Comment = Comment (if any)

This format is repeated for $1 \leq I \leq 35$. The value -1 has been inserted wherever a measurement is not applicable.

```
1
9
28., 0., 1119., 5600., 5600., 4., 3.
26., 2., 996., 5100., 5000., 22., 19.
24., 2., 1617., 8200., 8000., 52., 48.
22., 4., 1070., 5500., 5300., 46., 43.
20., 4., 1046., 5400., 5200., 49., 44.
18., 14., 1054., 5600., 5200., 100., 94.
16., 16., 1049., 5800., 5200., 160., 150.
14., 31., 1067., 6700., 5300., 410., 390.
10., 50., 1047., 9500., 5200., 1200., 1100.
2
6
28., 2., 1024., 5300., 5100., 72., 58.
24., 0., 1034., 5500., 5100., 120., 100.
20., 10., 1064., 5900., 5300., 160., 140.
16., 20., 1034., 6100., 5100., 290., 260.
12., 37., 1025., 8700., 5100., 1000., 1000.
20., 8., 1048., 5700., 5200., 150., 130.        $REVERSE CHECK
3
5
28., 0., 1023., 5100., 5100., 11., 10.
24., 0., 1029., 5200., 5100., 28., 24.
20., 2., 1025., 5500., 5100., 130., 120.
16., 13., 1057., 6100., 5200., 250., 230.
12., 51., 1030., 11300., 5100., 1800., 1700.
4
5
28., 2., 1036., 5200., 5100., 11., 9.
24., 6., 1083., 5500., 5400., 39., 31.
20., 2., 1032., 5600., 5100., 130., 120.
16., 7., 1027., 6400., 5100., 400., 380.
12., 44., 1026., 16200., 7600., 2600., 2500.    $IDS SLIP
5
5
28., 19., 21750., 1.2E5, 1.1E5, 430., 380.      $LONG RUN
24., 0., 1037., 5400., 5100., 76., 70.
20., 2., 1044., 5600., 5200., 140., 130.
16., 31., 1297., 7800., 6400., 420., 390.
12., 48., 807., 10000., 5100., 1600., 1500.     $IDS SLIP
6
5
28., 0., 1032., 5300., 5100., 45., 40.
24., 4., 1028., 5300., 5100., 67., 60.
20., 6., 1025., 5500., 5100., 130., 120.
16., 8., 1024., 6500., 5100., 420., 390.
12., 36., 1022., 11000., 5100., 2000., 1900.
7
5
28., 2., 1024., 5300., 5100., 60., 53.
24., 5., 1036., 5500., 5100., 95., 84.
20., 2., 1107., 5700., 5500., 56., 52.
16., 8., 1028., 6700., 5100., 460., 430.
12., 30., 1030., 13000., 5100., 2600., 2500.
8
5
28., 0., 1041., 5300., 5200., 30., 25.
24., 2., 1037., 5300., 5100., 33., 28.
20., 10., 1046., 5500., 5200., 90., 75.
16., 11., 1035., 6400., 5100., 380., 340.
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AD-A116 859 GTE SYLVANIA INC NEEDHAM HEIGHTS MASS F/G 17/2
HF WIDEBAND MODEM.(U)
APR 82 V ELLINS, P H ANDERSON, M N SANDLER F30602-79-C-0099
UNCLASSIFIED RADC-TR-82-85 NL

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12., 64., 1027., 10000., 5100., 1500., 1400.
9
5
28., 0., 1023., 5200., 5100., 34., 33.
24., 0., 1036., 5300., 5100., 48., 39.
20., 6., 1347., 7300., 6700., 170., 140.
16., 26., 1024., 6500., 5100., 410., 370.
12., 44., 1181., 14000., 5900., 2600., 2500.
10
4
28., 0., 1005., 11000., 10000., 440., 420.
24., 0., 1018., 12000., 10000., 640., 620.
20., 0., 1034., 13900., 10200., 1090., 1060.
20., 0., 1100., 1.4E4,  1.1E4,  690., 660.      $REVERSE CHECK
11
5
28., 91., 1981., 10000., 9900., 290., 270.
24., 42., 1035., 5800., 5100., 190., 180.
20., 186., 1060., 6200., 5300., 280., 270.
16., 320., 1028., 6400., 5100., 400., 380.
12., 759., 1055., 8300., 5200., 870., 820.
12
5
28., 8., 1142., 6600., 5700., 300., 290.
24., 2., 1102., 6500., 5500., 324., 310.
20., 12., 1039., 6400., 5100., 440., 380.
16., 24., 1031., 7400., 5100., 690., 640.
12., 55., 1024., 12000., 5100., 1700., 1700.
13
5
28., 0., 1022., 6000., 5100., 290., 280.
24., 6., 1027., 6300., 5100., 340., 330.
20., 12., 1046., 6500., 5200., 390., 370.
16., 24., 1022., 7200., 5100., 650., 620.
12., 54., 1071., 10000., 5300., 1600., 1500.
20., 10., 1028., 6000., 5100., 280., 270.       $REVERSE CHECK
14
4
28., 0., 1033., 6400., 5100., 410., 390.
24., 0., 1029., 6500., 5100., 450., 440.
20., 0., 1028., 7200., 5100., 630., 600.
16., 0., 1032., 9300., 5100., 1200., 1200.
15
4
28., 274., 1234., 4700., 4100., 200., 190.
24., 352., 1234., 4800., 4100., 220., 210.
20., 610., 1208., 5000., 4000., 300., 290.
16., 1542., 1229., 6100., 4000., 600., 550.
16
6
32., 2722., 1320., 4700., 3300., 420., 400.
28., 1487., 1320., 3700., 3300., 140., 130.
24., 3374., 1280., 4300., 3200., 330., 310.
20., 2311., 760., 5400., 1900., 830., 810.
24., 608., 1037., 2900., 2600., 100., 97.       $REVERSE CHECK
28., 1413., 2360., 7200., 5900., 420., 400.     $REVERSE CHECK
17
4
28., 7.4E4,  -1., 7000., 6100., -1., -1.
24., 7.2E4,  -1., 7000., 6100., -1., -1.                    1316-82
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20., 9.6E4,  -1., 7100., 6200., -1., -1.
16., 9.0E4,  -1., 7100., 6200., -1., -1.
18
4
28., 6700.,  -1., 8200., 6100., -1., -1.
24., 1.6E4,  -1., 8100., 6100., -1., -1.
20., 1.2E4,  -1., 8400., 6300., -1., -1.
16., 3.0E4,  -1., 8100., 6100., -1., -1.
19
5
28., 6700., -1., 12000., 6100., -1., -1.
24., 1.2E4, -1., 12000., 6200., -1., -1.
20., 5.6E3, -1., 12000., 6100., -1., -1.        $ANOMALY
16., 2.5E4, -1., 12000., 6100., -1., -1.
20., 1.8E4, -1., 12000., 6100., -1., -1.        $REVERSE CHECK
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28., 0., 1029., 5500., 5100., 120., 120.
24., 4., 1039., 5600., 5100., 130., 130.
20., 8., 1028., 6400., 5100., 400., 390.
16., 18., 1030., 7300., 5100., 670., 640.
12., 31., 1029., 11000., 5100., 180., 180.
21
5
28., 62., 17545., 1.E5, 8.7E4, 4000., 3600.      $LONG RUN
24., 16., 1026., 6200., 5100., 310., 280.
20., 7., 1045., 6600., 5200., 430., 390.
16., 27., 1031., 7700., 5100., 790., 730.
12., 55., 1023., 10000., 5100., 1800., 1700.
22
2
24., 0., 999., 10000., 10000., 170., 150.
0., 475., 8600., 5000., 1100., 1100.
23
4
28., 0., 1024., 5700., 5100., 190., 180.
24., 6., 1023., 5800., 5100., 230., 210.
20., 5., 1087., 6100., 5400., 210., 190.
16., 14., 1033., 8300., 5100., 970., 920.
24
3
28., 10., 1026., 6800., 5100., 540., 510.
24., 8., 1031., 7900., 5100., 900., 860.
20., 0., 1035., 6800., 5100., 530., 510.
25
4
24., 246., 1219., 6200., 4000., 650., 600.
28., 149., 1218., 5600., 4000., 440., 380.
20., 227., 797.,  -1., -1., -1., -1.
24., 148., 1021., 9500., 5500., 1200., 1100.     $REVERSE CHECK
26
3
24., 690., 1028., 5800., 2500., 990., 920.
28., 543., 1051., 6700., 2600., 1200., 1200.
32., 483., 1083., 6500., 2700., 1100., 1100.
27
4
28., 0., 1029., 5300., 5100., 58., 55.
24., 0., 1039., 5400., 5100., 67., 57.
20., 2., 1023., 5800., 5300., 140., 130.
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16., 0., 911., 7300., 4500., 890., 870.
28
3
28., 0., 1098., 5700., 5200., 65., 56.
24., 0., 1031., 5200., 5100., 33., 25.
20., 2., 718., 6900., 3500., 1000., 1000.
29
5
28., 0., 1031., 5400., 5100., 100., 100.
24., 0., 1039., 5570., 5100., 110., 110.
20., 2., 980., 6800., 4900., 510., 510.
16., 3., 1029., 7500., 5100., 770., 750.
20., 2., 1046., 6600., 5300., 420., 410.          $REVERSE CHECK
32
4
28., 2., 2313., 1.2E4., 1.1E4., 340., 330.
24., 0., 923., 6900., 4600., 370., 360.
20., 2., 1027., 6800., 5100., 530., 520.
16., 8., 1030., 7700., 5100., 840., 830.
31
4
28., 0., 1032., 5920., 5100., 240., 220.
24., 2., 1046., 5900., 5200., 220., 210.
20., 4., 1029., 7200., 5100., 680., 660.
16., 14., 1024., 10000., 5100., 1800., 1700.
32
4
28., 0., 1050., 5600., 5200., 130., 120.
24., 0., 1040., 6700., 5200., 510., 500.
20., 4., 1026., 6700., 5100., 520., 510.
16., 12., 1027., 10000., 5100., 1700., 1700.
33
3
28., 0., 960., 6800., 4700., 540., 530.
24., 0., 1040., 6500., 5200., 440., 420.
20., 2., 1043., 7500., 5200., 740., 720.
34
3
28., 0., 1035., 6600., 5100., 450., 440.
24., 2., 758., 6100., 3700., 620., 600.
20., 4., 733., 5100., 3700., 450., 440.
35
5
28., 0., 1028., 5200., 5100., 14., 8.
24., 2., 1039., 5300., 5100., 29., 20.
20., 4., 1060., 5800., 5300., 140., 110.          $REVERSE CHECK
20., 2., 1074., 6400., 5300., 300., 270.
16., 19., 1033., 7900., 5100., 790., 690.
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